Chemical Processing of Materials on Silicon: More Functionality, Smaller Features, and Larger Wafers

Nathan Marchack and Jane P. Chang

Department of Chemical and Biomolecular Engineering, University of California, Los Angeles, California 90095; email: jpchang@ucla.edu

Annu. Rev. Chem. Biomol. Eng. 2012. 3:235–62

The *Annual Review of Chemical and Biomolecular Engineering* is online at chembioeng.annualreviews.org

This article's doi:
10.1146/annurev-chembioeng-062011-080958

1947-5438/12/0715-0235$20.00

Keywords

integrated circuits, multifunctional oxides, atomic layer deposition, plasma etching

Abstract

The invention of the transistor followed by more than 60 years of aggressive device scaling and process integration has enabled the global information web and subsequently transformed how people communicate and interact. The principles and practices built upon chemical processing of materials on silicon have been widely adapted and applied to other equally important areas, such as microfluidic systems for chemical and biological analysis and microscale energy storage solutions. The challenge of continuing these technological advances hinges on further improving the performance of individual devices and their interconnectivity while making the manufacturing processes economical, which is dictated by the materials' innate functionality and how they are chemically processed. In this review, we highlight challenges in scaling up the silicon wafers and scaling down the individual devices as well as focus on needs and challenges in the synthesis and integration of multifunctional materials.

INTRODUCTION

The famous Moore's law that has become the guiding principle of integrated circuit (IC) fabrication was first published in 1965 (1). Its bold vision, which projects the exponential growth of IC packing density, was in the same spirit as Feynman's lecture on "There's plenty of room at the bottom" (2). Over the past two decades, both top-down and bottom-up approaches have significantly matured, which has led to many scientific and technological advances at the nanometer scale beyond electronics, including microfluidic systems for chemical and biological analysis (3–6) and microscale energy storage devices (7, 8). However, as Moore's Law approaches its end based on conventional metal-oxide-semiconductor field effect transistors, novel materials and architectures are in great demand to realize the projected increase in devices' functionality and speed while reducing the devices' weight and energy consumption. The ultimate challenge for chemical processing of materials in silicon-based devices is to enable, simultaneously, cost-effective dimensional and functional scaling. This dictates the design and discovery of new materials with multiple functionalities, novel synthetic processes with atomic precision control over large wafers, and high-fidelity assembly or patterning of these materials into complex structures. This article first discusses the challenges in upscaling of the wafer and downscaling of the individual devices, which motivate the following section on the needs and challenges in realizing multifunctional materials, and then describes the development and advancement in atomic layer deposition (ALD) and plasma-enhanced patterning processes as enablers to integrate these new materials into ever more complex structures to deliver the desired device performance.

Challenges in Upscaling: Economy of Scale

The logic behind scaling up the silicon wafer is based mainly on the economy of scale. Given that current IC manufacturing consists of more than 800 process steps (9) and assuming that each process step has a yield of 99%, the overall yield at the finish line of a fully processed silicon wafer would be an unacceptably low 0.03%. If an overall yield of 99% is required, each process step needs an incredibly high yield of 99.999%. This requirement has resulted in the necessary use of a clean room, the production of ultrahigh-purity specialty chemicals and water, the development of extremely sophisticated vacuum reactors, the implementation of highly automated robotic systems, and the training of qualified personnel. As these capital equipment and human resource investments have skyrocketed over the past two decades, there is a major economic gain if a much larger wafer (from which many more functional chips can be produced) can be processed, assuming that no significant cost increase occurs. This has led to the transition of silicon wafers from 2 inches to 12 inches (300 mm) in diameter over the past 60 years. If a chip size is nominally the same regardless of the diameter of a wafer, then an increase in the wafer area by a factor of 36 could be expected to result in a similar order of magnitude increase in chip production at the same or a similar throughput. As shown in **Figure 1**, as the wafer diameter increases, the wafer thickness and number of attainable chips increase, whereas the corresponding feature sizes have consistently decreased. The enabling factors contributing to the upsizing of the wafer and downsizing of the features include basic research on and technological breakthroughs in many unit operations used in IC fabrication: a much improved crystal growth process for large-diameter silicon (10, 11); a thorough understanding of the dopant distribution, control, and diffusion processes (12–14); advancement in photolithography and photoresist design (15–17); complex wafer cleaning strategies (18, 19); a deeper understanding of the transport and kinetics issues involved in designing larger-scale reactors for thin-film deposition/etching (20, 21); and advanced heat treatment to minimize the thermal budget (22).

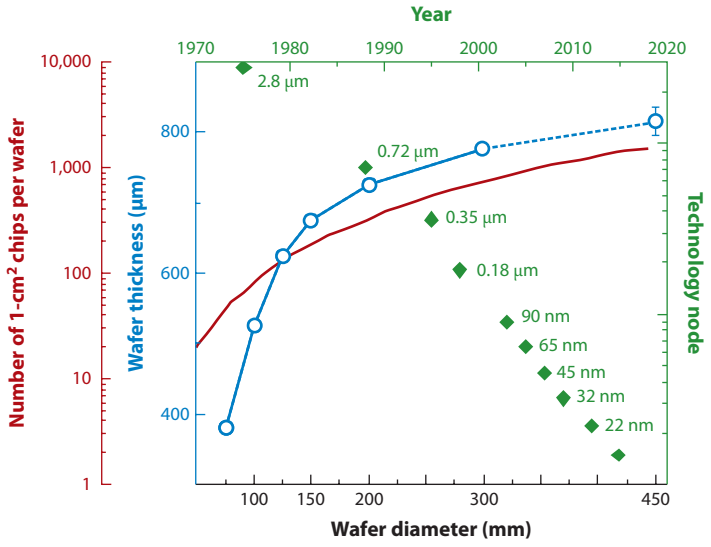


Figure 1

The number of 1-cm^2 chips per wafer as a function of increasing wafer size from 4 inches to 12 inches and beyond. The dashed line shows the extrapolated estimate for an 18-inch wafer. The corresponding wafer thickness and the technology nodes over the past 50 years are also shown (figure adapted from References 23, 140).

So, is it ever possible to go into production with the 18-inch (450 mm) silicon wafers that first debuted at Semiconductor Equipment and Materials International Conference West (SEMICON West) in 2006? Silicon, as the second most abundant element on earth, has surpassed all other semiconductors in prominence and dominated the electronic industry, partly owing to the relative ease of its crystal growth and its availability. The International Technology Roadmap for Semiconductors (23) has indicated that the next-generation wafer size, 450 mm, is to be introduced in 2012, but it was evident, as at the recent 2011 SEMICON West meeting, that a transition may occur much later, in 2016–2019. The reasons for the delay lie beyond the need to overcome technological challenges related to growing a larger single-crystal silicon ingot and the fact that larger and thicker silicon wafers are more brittle and have more defects. The real challenge traces back to what motivated the wafer size upscaling: the economics. In this highly competitive industry, synchronized planning is the key to the success of this projected transition. For example, to maintain the overall process yield and throughput while continuing to improve the uniformity of processing output over a larger area, all equipment must be further upsized, which is technologically possible but a costly endeavor. The bottom line on when and if 450-mm production occurs is the return on investment, as is the case in all successful industrial sectors (24).

Challenges in Downscaling: Functionality and Performance of Smaller Features

The aggressive downscaling of transistor devices mandates the introduction of new materials and device architectures to realize the projected increase in device functionality and speed while reducing their weight and energy consumption. The basic building block of the electronic industry is a metal-oxide semiconductor (MOS) field-effect transistor, as depicted in **Figure 2**. The metal modulates the conductivity of the silicon (semiconductor) through an insulator (oxide), and the on-off of this device is used as the 1 and 0 binary code for computation. The physical dimensions

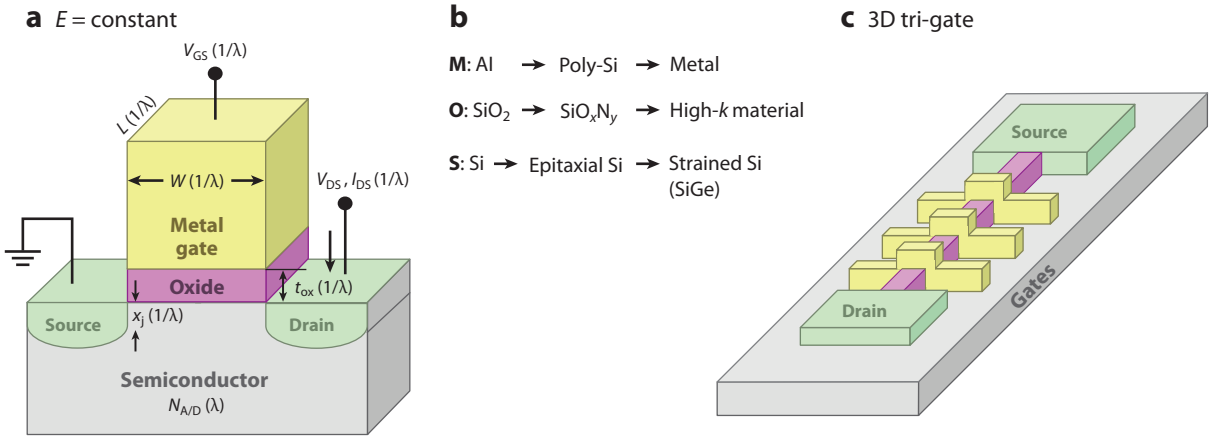


Figure 2

(*a*) A simplified cross-sectional view of a metal-oxide semiconductor field-effect transistor; key parameters are labeled along with their constant-field scaling factor (λ). L, W, t_{ox}, and x_j are the gate length, width, dielectric thickness, and junction depth, respectively. V_{GS}, V_{DS}, and I_{DS} are the gate voltage, drain voltage, and drain current, respectively. $N_{(A/D)}$ is dopant concentration, and E is the electric field. (*b*) The material evolution and (*c*) the geometric advancement of a 3D tri-gate structure to further enable device scaling.

of this device have been aggressively downscaled over the past few decades to improve speed and packing density. One classic scaling methodology is constant-field scaling (25), which keeps the electric field in the transistor unchanged by reducing the supply voltage and the transistor length, oxide thickness, and junction depth while increasing the doping level in the channel by the same factor. This device downscaling has resulted in the greater performance, lower-cost (per transistor), and more energy-efficient electronic devices that have shaped today's technological landscape. In simple terms, smaller is faster and better. However, as device dimensions were further reduced below 90 nm, novel device architecture and much thinner but compositionally tailored materials were required to achieve the desired functionality. Over the past decade, the incorporation of strained silicon (26, 27), high-*k* dielectrics (28), and metal gates (29) has enabled channel mobility improvement and the scaling of gate capacitance, which has essentially redefined the material systems to be used in future MOS devices. More recently, the introduction of a tri-gate structure was considered a revolution, as it provided one additional degree of freedom in device scaling by changing the core structure of the transistor from a planar one into a three-dimensional one, thereby enabling further device scaling based on Moore's law while achieving significant energy savings (30). The 3D architecture and novel materials are likely to shape the landscape of future transistors, including the potential use of carbon nanotubes and polymers on the basis of their unique properties (31, 32).

MULTIFUNCTIONAL MATERIALS

Silicon was not the substrate material of choice when the transistor was first invented. What set silicon apart from other semiconductors and made it the dominant material in IC device fabrication was that it can be easily oxidized to form a high-quality dielectric layer (SiO_2) with an interface superior to that of any other semiconductor. This became a classic example of processing advantages outweighing innate material properties in the selection and integration of materials. For many decades, advancement in the field focused on circuit design and wafer scaling, with little

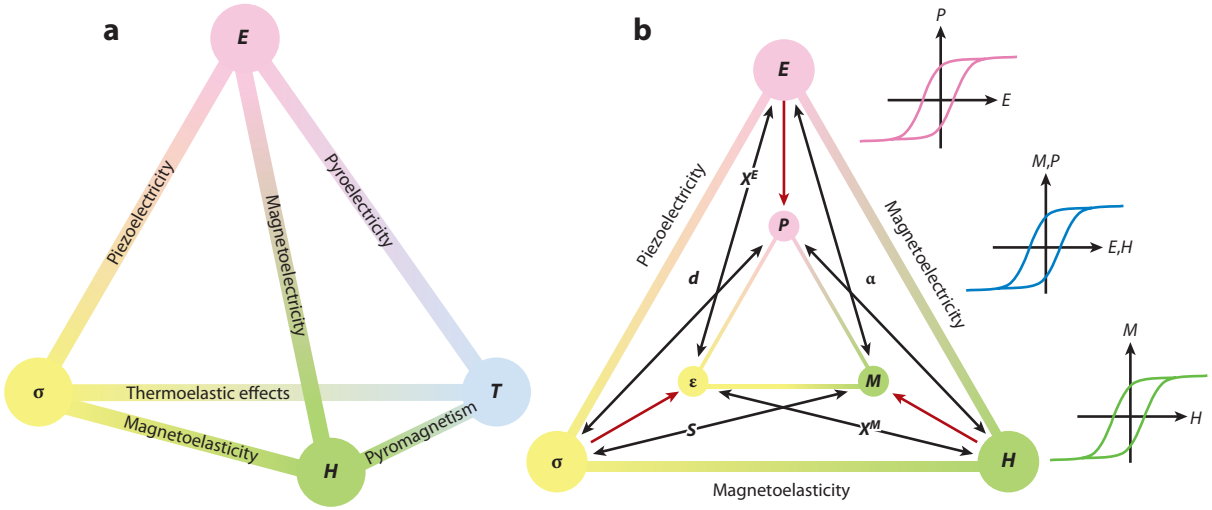


Figure 3

(*a*) Heckmann diagram showing the interplay between the thermal, mechanical, electrical, and magnetic properties of a material. (*b*) Heckmann diagram showing specifically the magnetoelectric coupling and the attainable magnetic response to an electric field as well as the modification of polarization by a magnetic field,, where *E*, *H*, *T*, *S*, *X*, *P*, *d*, and *M* are the stress, electric field, magnetic field, temperature, strain, piezoelectric/magnetic coefficient, electric polarization, displacement, and magnetic polarization, respectively. Adapted from References 33, 141.

to no new material introduction. A paradigm shift started about a decade ago, when the scaling of this SiO_2 layer was projected to reach less than 10 Å, at which direct quantum-mechanical tunneling would result in an unacceptably high leakage current and dielectric breakdown would happen at intolerably low voltages. This issue dictates the design and development of complex metal oxides. To rationally design and tailor these materials for their intended applications, this section highlights the basic scientific considerations and their ongoing and future impact in both logic (high-*k* dielectrics) and memory (multiferroics) devices.

As shown in the expanded Heckmann diagram in **Figure 3*a***, the thermal, electrical, magnetic, and mechanical properties of materials are coupled through axial tensor relationships (33). As these properties can be closely related and described by reference to equilibrium states, by controlling the atomic arrangement of the materials and their interfaces, material properties can be tuned over a wide spectrum to realize unique characteristics, such as ferroelectricity (34, 35), piezoelectricity (36, 37), and magnetoelectricity (38), which in turn lead to applications in nanoelectronics (39, 40), optoelectronics (41, 42), photonics (43, 44), spintronics (45, 46), and sensors (47, 48). One class of materials that holds promise to enable further device scaling, provide more material functionalities, and realize potential new applications is the complex metal oxide discussed earlier, as it provides the ultimate playground for the exploration of the coupling and interplay among the charge, spin, orbital, and lattice degrees of freedom (49–52). By controlling the composition and microstructure of the complex metal oxides, the aforementioned interactions can lead to novel ground states for the system that can be manipulated by external perturbations (49). In this section the discussion is focused on complex metal oxides and their application as both high-*k* and magnetoelectric materials (**Figure 3*b***); however, the same principles and considerations are applicable to the design and integration of various multifunctional materials combined with other factors, such as thermoelectrics.

Complex Metal Oxides as High-*k* Materials

The engineering of complex metal-oxide thin films at an atomic level has seen great success with the introduction of high-*k* materials in the transistor structure. Metal oxides are superior to SiO_2 in terms of their higher dielectric constants, which enable them to supply heightened capacitance while simultaneously providing a physically thicker layer to suppress quantum mechanical tunneling and dielectric breakdown (53). Hafnium-based materials have emerged as the designated dielectrics in nanoelectronics with a gate length less than 45 nm, and the implementation of a non-silicon-based gate dielectric means a paradigm shift from diffusion-based thermal processes to ones based on ALD. Complex metal oxides are needed in high-*k* applications because a simple binary metal oxide does not have a better interface with Si compared with SiO_2. The chemical potential difference across the interface drives chemical reactions (54), and the lack of an oxygen diffusion barrier typically results in the formation of a SiO_2-rich layer at the interfaces of the oxide with both the Si substrate and the polysilicon gate. These interfacial layers degrade the attainable capacitance of the gate dielectric layer, which often results in an increased interface state density. The other issue with simple binary oxides is that they crystallize at relatively low temperatures, 500–700°C, and thus undergo thermally induced crystallization at typical postdeposition annealing temperatures. This leads to increased leakage current and dopant diffusion across the dielectric grain boundaries as well as threshold voltage instability owing to charge trapping (55).

To alleviate these concerns, complex metal oxides based on hafnium have been explored, as they possess the desired characteristics of each constituent binary oxide. For example, to address the interfacial issues, hafnium silicate (based on HfO_2 and SiO_2) has significantly better thermochemical stability owing to the reduced chemical potential difference to Si with the inclusion of SiO_2 (**Figure 4*a***) (56, 57). Hafnium aluminate (based on HfO_2 and Al_2O_3) is another promising material, as Al_2O_3 is a well-known oxygen diffusion barrier that protects the Si surface from oxidation and is thermodynamically stable in contact with Si (58, 59). To suppress the low-temperature crystallization process, a strategy is to form an alloy of HfO_2 with a good glass former (SiO_2 or Al_2O_3) to achieve an amorphous structure that can be stabilized at high temperatures. Although this approach lowers the overall dielectric constant, it results in an amorphous microstructure with enhanced phase stability and lower trap densities as compared with the binary oxide counterparts. Another strategy is to find an oxide that has a small lattice mismatch with silicon so that it can be grown as a single crystalline material that can withstand high temperatures and provide a high-quality interface; an example is hafnium lanthanate (based on HfO_2 and La_2O_3) (60). These promising hafnium-based multicomponent oxides including Si, Al, and La elements have relatively high permittivity, wide bandgap, high thermal and chemical stability, and large band offsets to silicon (61), as summarized in **Figure 4*b***. In addition, by varying the fraction of oxygen or nitrogen during deposition, these compounds can also be designed to improve electric properties (62, 63).

Multiferroics for Memory Applications

In addition to the aggressive downscaling of nanoelectronics, nanoscale electromagnetic devices are emerging as enablers to realize advanced logic and memory devices, especially ones that require less energy to write and store information and result in less energy dissipation. The ability to electrically control magnetism in a solid-state material has been a challenge for the past century but became attainable with the development of multiferroic materials in recent years. The coexistence of several order parameters in a multiferroic material yields novel physical phenomena and offers possibilities for new device functionalities. This allows for further technological advancement in areas, such as computer memory, that are critical for realizing the full potential of handheld devices

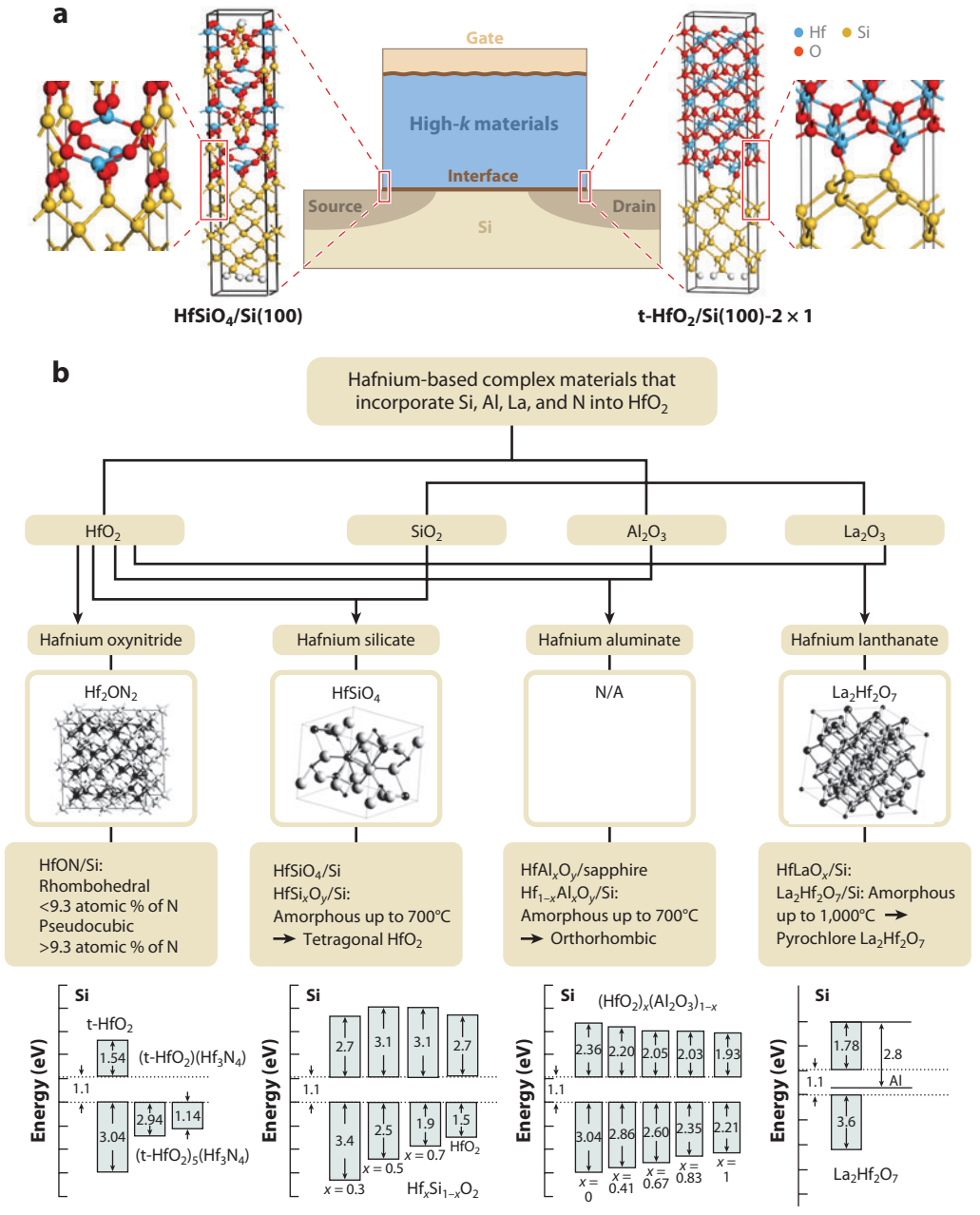


Figure 4

(*a*) A schematic cross-sectional view highlighting the complexity at the interface between a high-*k* material and silicon. The relaxed crystal structures for two possible interfaces are displayed: (*left*) $HfSiO_4$/Si(100) and (*right*) tetragonal (t)-HfO_2/Si(100)-2 × 1. Figure adapted from Reference 61. (*b*) A summary of Hf-based complex oxides that illustrates material tunability and design approaches.

(e.g., smart phones, medical devices). Specifically, a single-phase multiferroic is a material that exhibits at least two ferroic order parameters of the following: ferroelectricity, ferromagnetism, ferroelasticity, or antiferromagnetism (64). Among all possible combinations, the strong coupling between magnetic and electronic order parameters has gained the most attention recently. The ability to produce a magnetic moment by an external electric field and vice versa, as shown in **Figure 3*b***, especially if such control is attainable at near room temperature (49–51, 65), provides an additional degree of freedom in the design of new devices such as spin-field-effect transistors (66, 67) and advanced memory devices (68, 69) that could offer fast and low-power electrical write operation and nondestructive magnetic read operation. Despite the array of promising features for multiferroic materials, several challenges must be overcome, namely that few single-phase, intrinsic materials exhibit multiferroic properties, and only one material discovered thus far, $BiFeO_3$, displays these properties at room temperature (70). Because the ultimate goal for practical device application of multiferroic materials is attainable only by strong coupling between different types of ferroic order, more degrees of freedom for this strong magnetoelectric coupling to occur are highly desirable. Similar to the advances in 3D transistor structures, geometric design becomes an enabling factor to combine ferromagnetic and ferroelectric materials to form composite multiferroics that can potentially serve as a platform for novel logic and memory devices (71–73).

One way to create composite multiferroic material systems is to integrate ferroelectric and ferromagnetic materials through interfacial strain effects to achieve magnetoelectric coupling. The remarkable potential of these materials is based on the product of the magnetostrictive effect in the magnetic phase and the piezoelectric effect in the piezoelectric phase. Horizontally aligned materials such as nanolaminates with alternating layers of piezoelectric and ferromagnetic materials are the easiest to conceptualize, as shown in **Figure 5*a*** (50). This connectivity scheme is classified as a 2–2 configuration and can be realized by thin-film growth processes (74). With this setup, when a magnetic field is applied to a composite, the magnetic phase changes its shape through magnetostriction, and the corresponding strain is passed to the piezoelectric phase to cause electrical polarization. Similarly, the piezoelectric response of the ferroelectric material in an applied field can cause strain at the interface with the ferromagnetic material, which results in a piezomagnetic response that generates a change in magnetization or magnetic anisotropy (49). However, the substrate clamping effect limits the amount of piezoelectric strain, thereby limiting the attainable magnetoelectric effect (75). As a result, vertically aligned structures such as nanorods embedded in the matrix of another phase have also been explored (**Figure 5*b***). This 1–3 configuration has a huge surface area-to-volume ratio, which allows for a higher attainable magnetoelectric coefficient (76, 77). More recently, the 0–3 configuration, shown in **Figure 5*c*,** has also been explored as an alternative way to create closely coupled synthetic multiferroics in which one phase fills the pores formed by another (78). Because of the flexibility of the porous phase, unique strain states can be realized, and much closer coupling is expected. Although self-assembly of nanocomposites has been examined with promising outcomes, to realize large-scale processing and integration, it is more effective to create and control the geometry of one phase (via patterning or self-assembly) followed by interface formation with another phase. As shown in **Figure 5**, the time progression for synthesis of these composite materials dictates a highly uniform and conformal thin-film coating process to realize the close coupling between the piezoelectric and ferromagnetic phases.

ATOMIC LAYER DEPOSITION

ALD (79–81) is typically described as a binary chemical reaction sequence in which the surface reaction of each chemical precursor is self-limiting (82–86). Two main features that distinguish

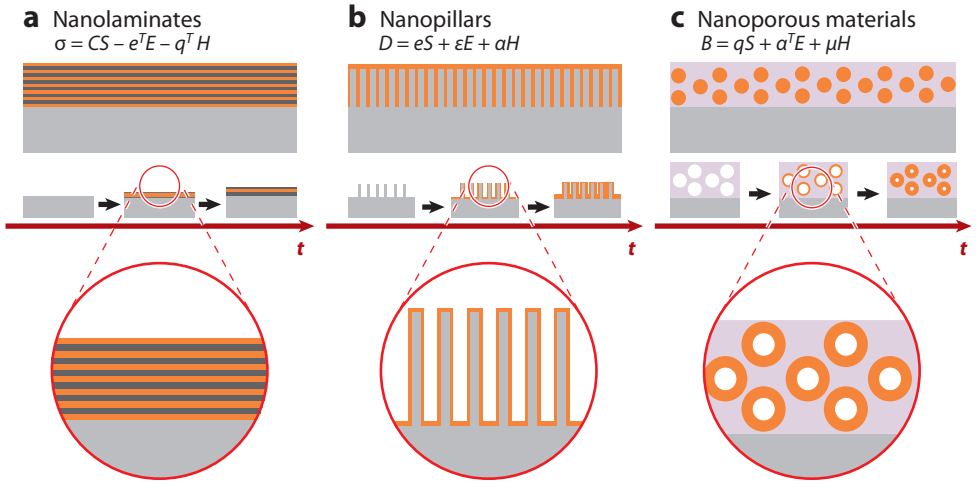


Figure 5

Schematics of heterostructures with different connectivity schemes, including (*a*) nanolaminates, (*b*) nanopillars, and (*c*) nanoporous materials. The time progression of the materials synthesis highlights the importance of a uniform and conformal coating to realize the intimately coupled interfaces in these complex structures. The constitutive equations describing the mechanical-electric-magnetic response in these heterostructures are (50): $\sigma = c\,S - e^T E - q^T H$; $D = e\,S + \varepsilon E + \alpha H$; $B = q\,S + \alpha^T E + \mu H$, where σ, S, D, E, B, and H are the stress, strain, electric displacement, electric field, magnetic induction, and magnetic field, respectively; c, ε, and μ are the stiffness, dielectric constant, and permeability, respectively; e and q are the piezoelectric and piezomagnetic coefficients; and α is the magnetoelectric coefficient. The superscript T means the transpose of the tensor.

ALD from other chemical processes are: (*a*) the deposition process comprises a sequence of discrete self-limiting process steps, and (*b*) each self-limiting step must lead to a monolayer saturation.

The reaction kinetics for each sequence involves several gas-surface interactions that include: (*a*) adsorption of the precursor molecules onto the substrate, (*b*) surface reaction, and (*c*) desorption of the reaction products or by-products. Typically, low-temperature and mildly oxidizing processes are required for ALD to avoid pyrolyzing the precursor or oxidizing the interface between the deposited materials and the substrate.

To control the ALD process, the starting surface must be treated to generate the desired functional groups necessary to initiate the reactions. This process is sometimes referred to as surface activation. Because H_2O is commonly used as an oxidant in ALD, it is often desirable to activate the surface with H_2O to generate hydroxyl groups on the surface (–OH). These surface hydroxyl groups serve as reactive sites for subsequent chemical reactions. This initialization step can take several chemical pulses to complete owing to the steric hindrance effect and the activation energy required for the reaction to occur. This is sometimes observed as an incubation time before the layer-by-layer growth begins. If the surface is not properly activated, nucleation processes can occur on defect sites, and the nonvolatile reaction products can redeposit at these seeding sites to form islands. As the deposition proceeds, these islands grow into grains, which finally coalesce into films that are usually neither uniform nor continuous. Without surface activation, ALD films grow inconsistently with significant texture and roughness (87).

Using the deposition of a complex metal oxide as an example, upon surface activation, a volatile and thermally stable metal-organic precursor (ML_x: M represents a metal, and L is a molecular ligand that makes ML_x volatile) is first introduced to react with the surface functional group and

form a saturated monolayer with M–O bonds. During this process, a volatile product (LH) is formed and leaves the surface:

$$-\mathrm{OH} + \mathrm{ML}_x \rightarrow -\mathrm{O}-\mathrm{ML}_{x\text{-}1} + \mathrm{LH}$$

Once all the –OH groups are consumed and the surface is terminated with the L ligands, no more surface reaction occurs. An oxidant (H_2O or O, O_2, O_3, H_2O_2) is then introduced to remove the remaining organic ligands, form LH as the volatile product, and regenerate the surface hydroxyl groups as well as form the –O–M–O– bonds that are the building blocks for complex metal-oxide materials:

$$-\mathrm{O} - \mathrm{ML}_{x-1} + (x-1)\mathrm{H_2O} \rightarrow -\mathrm{O}-\mathrm{M}-(\mathrm{OH})_{x\text{-}1} + (x-1)\mathrm{LH}$$

An important observation is that, at this time, the surface is almost restored to its initial state after the surface activation. This sequence of surface reactions that restores the surface to its starting point is known as one ALD deposition cycle. This restored surface activity allows the sequential reactions to occur and complete subsequent ALD cycles. However, because more than one –OH can be formed per metal atom at this stage, the restored surface is not exactly the same as the initially activated surface. Thus, the region of transition from the substrate to the complex metal oxide film may have a slightly different density and deposition rate per cycle when compared with the bulk material. Furthermore, not all of the hydroxyl groups serve as subsequent reaction sites for the metal-containing precursors owing to the steric hindrance effect. Some of these –OH groups may react to eliminate water, and this dehydroxylation process can reduce the density of available –OH groups. In addition, the process of losing excessive –OH ligands by dehydroxylation is responsible for cross-linking and can result in more densely packed and higher-quality films.

Once complete surface coverage of the initial atomic layer occurs, the deposition thickness scales linearly with the number of deposition cycles. Because each half reaction is self-limiting, growth of the thin film beyond one monolayer is not possible once all of the surface functional groups have reacted. Thin films are thus deposited by repetitive application of a single-layer deposition sequence (or less than a layer owing to the steric hindrance of the precursor molecules), and the two chemical pulses (H_2O and ML_x) can be varied independently in terms of their duration and concentrations (pressures). Control of the number of pulsing cycles allows one to manipulate the spacing of a nanolaminate structure with a resolution of ~3 Å. Importantly, it is also possible to achieve ALD from a single self-limiting chemisorption process. In this case, the precursor molecules chemisorb, saturate the surface, and subsequently exchange their ligands with another precursor molecule to start forming the film. The creation of a complex nanolaminate superlattice structure can then be realized with an appropriate selection of precursor chemicals and cycles. In this way, multiple metal precursors can be introduced to synthesize complex metal oxides of different compositions. Because the basics of ALD of high-*k* materials have been discussed in Volume 2 of this Annual Review (9), the following discussion focuses on ALD processing advantages and adaptability for growing complex metal oxides on planar surfaces and 3D nanostructured templates to form engineered composite multiferroics.

Atomic Precision and Larger Area

Because ALD is based on specific surface reactions, the corresponding reactor design is much simpler compared with other chemical vapor deposition (CVD) processes, as the gas flow pattern does not play an important role except for optimization of the wafer throughput. This means the

reactor can be more easily scaled up to accommodate 450-mm wafers in the future. In general, the formation of a steady-state adsorption wave between the substrates during a precursor pulse depends strongly on the sticking probability and diffusion coefficient, the mean flow rate of the carrier gas, and the reactor temperature. However, the deposition rate per cycle of most ALD processes is temperature dependent, and thus uniform temperature control is still critical. By controlling the reactor temperature, chemical pulse time, chemical purge time, and total number of ALD cycles, desired thin-film thicknesses can be achieved. The typical sticking probability of the precursor molecules is between 0.0001 and 0.1. Based on a typical ALD deposition rate of ~0.5–3 Å/cycle and a typical desired thin-film thickness of ~1–20 nm, approximately 5 to 100 ALD cycles are required to deposit the desired complex metal oxides. To meet the throughput target of >10 wafers per hour (88), approximately 3–5 minutes are available for each wafer, including wafer loading and unloading. Thus, short ALD cycle time and purge time (hundreds of milliseconds) are required, which remains an engineering challenge. Although ALD usually has a lower processing temperature than CVD processes, sometimes the lowest processing temperature is not sufficient to avoid damage to the sample, or the ALD growth temperatures for different precursors may not overlap. To address these challenges, radical-enhanced ALD (RE-ALD) has been used as an effective alternative, as the highly reactive species from a plasma allow the surface reaction to take place at lower and similar temperatures (89, 90), as shown in **Figure 6**.

An exciting application for ALD is the synthesis of complex metal oxides such as multiferroic thin films, though some other thin-film growth methods have been applied to this task. Some key aspects in the synthesis of multiferroic materials include the control of the identity, placement, and function of every important element in the intrinsic multiferroic material as well as the further control of the interfaces in an extrinsic materials system. (50). For $BiFeO_3$, for example, pulsed laser deposition (PLD) has been the primary synthetic method (49), as it has outstanding characteristics for the epitaxial growth of films. The disadvantages, however, include the difficulty of deposition over large substrates, and conformal coating over 3D nanostructures remains a challenge owing to the plume-like ejection of species from the target. ALD is a complementary method that draws its strengths from specific surface reactions that can deposit highly conformal films with outstanding uniformity and composition control. PLD and ALD are inherently different, as one is a physical and the other is a chemical process. ALD also allows the local composition/bonding arrangement to be varied, even if the overall stoichiometry remains constant. Specifically, the lateral and vertical distribution of a given element can be tailored, the former through the steric hindrance effect of the precursor molecules used and the latter through the frequency of alternating ALD cycles (90). By realizing the control of composition and atomic arrangement, the conformality attainable by ALD allows nanostructured composite material systems to be synthesized.

Conformal Coating for Complex Nanocomposites

The conformality unique to ALD processing offers an additional degree of freedom in designing multiferroics by achieving uniform and closely coupled interfaces between the two phases. Although self-assembled piezoelectric and ferromagnetic composites have been formed by PLD, using lithographically patterned structures or mesoporous templates followed by ALD offers a complementary solution to synthetically controllable architectures. An example is the synthesis of the piezoelectric material $Pb(Zr_{0.5}\ Ti_{0.5})O_3$ (PZT) (91) via ALD over a mesoporous cobalt ferrite (CFO) material formed by evaporation-induced self-assembly (92). As shown in **Figure 7**, to achieve the optimal piezoelectricity, an ALD deposition sequence of (Pb-O)-(Ti-O)-(Pb-O)-(Zr-O) controlled the PZT composition at metal-atomic ratios of Pb:Zr:Ti = 2:1:1. The growth rate of PZT was determined to be 0.7 nm/cycle, and film thicknesses of 6–12 nm were achieved by

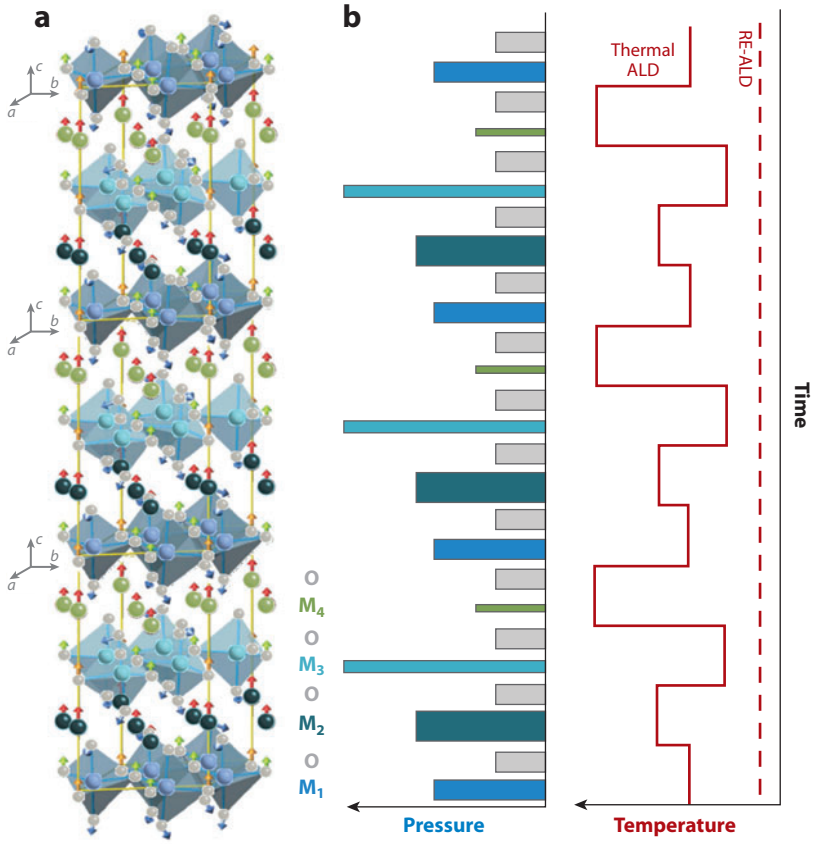


Figure 6

(*Left*) Schematic illustration of atomic layer deposition (ALD) utilization to control the deposition of constituent metal oxides leading to the formation of a complex metal oxide. (*Center*) The chemical pulses of multiple metal precursors (M_x) and an oxidant (O). (*Right*) The temperature profiles needed for thermal (stepwise, *solid line*) versus radical-enhanced (constant, *dashed line*) ALD (RE-ALD) processes. A constant temperature profile attainable with RE-ALD allows for deposition of materials of disparate precursor volatilities.

repeating the ALD cycle sequence. Mesoporous CFO thin films with a pore diameter of approximately 14 nm were used as a template for PZT growth to form a 0–3 nanostructured multiferroic composite. Scanning electron microscopy analysis confirmed that the coating was uniform and conformal over the interior surface of the pores. As a result, a higher coercive magnetic field (H_c) and a lower saturation moment (M_s) were achieved with PZT/CFO than with an identical CFO sample. The result of this 0–3 configuration is on par with or superior than those reported in literature, including those for the 2–2 and 1–3 configurations (F. Zhang, T. Quickel, S. Tolbert, and J.P. Chang, in preparation).

PLASMA-ENABLED PATTERNING

As advanced transistors begin to dictate the use of novel, complex materials such as multiferroic and electroceramic oxides, the challenge of matching patterning fidelity standards for these substances

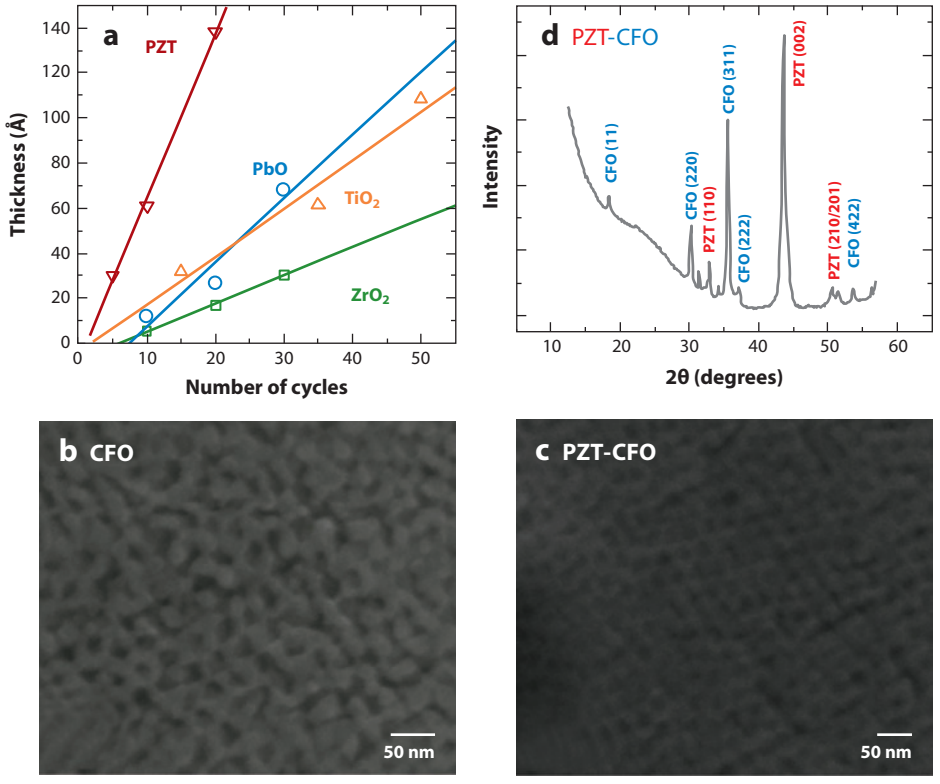


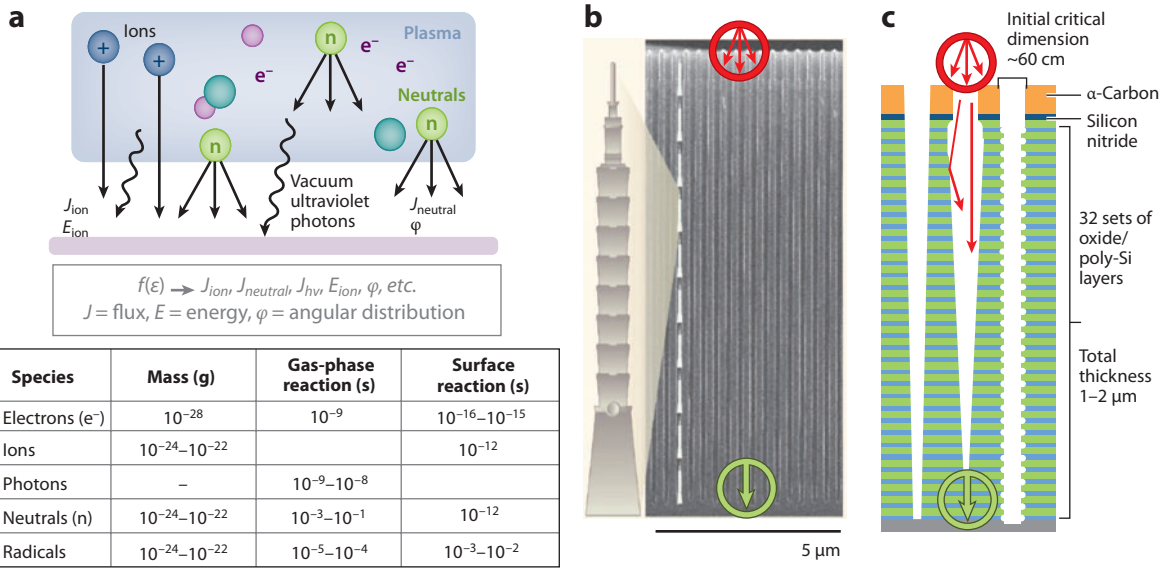
Figure 7

(*a*) Atomic layer deposition growth rate of $Pb(Zr_{0.5}\ Ti_{0.5})O_3$ (PZT) in comparison with that of its constituent oxides. (*b*,*c*) Scanning electron microscopy images of (*b*) mesoporous cobalt ferrite (CFO) thin films and (*c*) a PZT-CFO sample. (*d*) X-ray diffraction patterns of PZT-CFO thin films that confirm their respective crystal structures.

to those of well-studied systems such as Si and SiO_2 becomes imperative. So far, the most successful method of patterning materials is a combination of optical lithography and plasma etching, which has been demonstrated successfully for a wide variety of materials such as semiconductors, oxides, and metals (93, 94). Although there have been reports on bottom-up and self-assembly-based approaches to generate nanoscale patterns, such as by area-selective ALD (95, 96), this section discusses the potential use of top-down processing methods to create highly ordered nanopatterns at resolutions less than 14 nm and also highlights limitations that must be overcome to ensure the success of these processes.

Smaller Features and Higher Aspect Ratios

In top-down patterning methods, structures are created by selectively removing unwanted material, each time from the layer furthest away from the substrate. At the length scales of current and future transistor devices, precise control over the anisotropy of the etch process is of paramount importance, as even minimal deviation from the pattern layout can cripple device performance. For this reason, application of a partially ionized gas, or plasma, has been the primary technique used in the past few decades for micro- to nanoscale patterning of semiconductors,



Species	Mass (g)	Gas-phase reaction (s)	Surface reaction (s)
Electrons (e^-)	10^{-28}	10^{-9}	10^{-16}–10^{-15}
Ions	10^{-24}–10^{-22}		10^{-12}
Photons	–	10^{-9}–10^{-8}	
Neutrals (n)	10^{-24}–10^{-22}	10^{-3}–10^{-1}	10^{-12}
Radicals	10^{-24}–10^{-22}	10^{-5}–10^{-4}	10^{-3}–10^{-2}

Figure 8

Challenges in controlling plasma etching outcomes. (*a*) Species and key parameters in a plasma with their respective mass and time scales. Purple and teal spheres indicate etching and depositing spheres in the plasma. (*b*) High–aspect ratio trenches in relation to one of the world's tallest freestanding structures, Taipei 101, and (*c*) possible etch profile defects (tapering in the two trenches on the left and scalloping in the rightmost trench) in such features with the incorporation of multilayered composite films. Panels *a* and *c* adapted from Reference 142; panel *b* adapted from Reference 100.

oxides, nitrides, metals, and polymers (97). Plasmas are the fourth state of matter and contain several different species, namely, charged ions and electrons, metastable and reactive neutrals and radicals, and photons, as depicted in **Figure 8*a***. This wide variety of species forms a unique nonequilibrium environment in that the electron temperature is substantially higher than the average ion temperature, which is greater than the gas temperature ($T_e \gg T_i > T_g$). Considered separately, each of these species is usually insufficient to achieve the desired and directional reactions with the surfaces to be treated, but when they are supplied simultaneously to the surface with sufficient fluxes and desirable ratios, a wealth of well-controlled reactions becomes attainable (98, 99). As illustrated in **Figure 8**, when a voltage is applied to the sample, the voltage bias allows for directional control of reactive ionic species to the surface. As the ion impacts create reactive sites on the surface, other impinging plasma species can react readily with the surface materials to form volatile etch products. Because of the energetics of the reactive species in the plasma, surface reactions usually possess minute activation energies, thereby circumventing the need for intensive and potentially damaging substrate heating. However, because of the distinct nature and reactivity of each plasma species, their interplay poses great challenges as the dimensions of the features to be transferred approach the size of molecules or even atoms.

On the other side of the spectrum, achievement of a sufficiently fast etch rate while maintaining anisotropy and low damage has been a concern for the high–aspect ratio features (≡ depth/width) that certain applications demand, e.g., advanced memory devices, as illustrated in **Figure 8*b***(100). Within such features, the ratio of the neutral and ion fluxes as well as the ion incident angle change dynamically as the aspect ratio increases during patterning. These changes have significant effects on the etch yield, which is a dimensionless measurement of the number of

atoms removed normalized to a selected incoming etchant species. Because the etch yield dictates material removal within the feature, the aforementioned parameters clearly play a significant role in achieving the desired profile evolution. The situation is further complicated as new materials such as magnetic materials and complex metal oxides emerge for additional applications, as maintaining high degrees of specificity dictates a delicate balance between the desired outcome and the viable etch chemistries (101). For example, the chemistries that are required to etch an organic polymer compound (such as a photoresist) and a complex metal oxide are markedly different. **Figure 8*c*** shows a schematic diagram of such a device and possible profile defects such as tapered sidewalls, undercutting, and notches caused by preferential etching of certain layers (102–105).

Thermodynamic and Kinetic Framework

The challenge of executing the high-fidelity patterning of complex devices is a nontrivial task, in no small part owing to the large disparity in length and timescales between the various regimes involved in a plasma etch process. Length scales span from the reactor scale (centimeter) to topographical features (micrometers to nanometers) down to molecules and atoms on the surface (<nanometers), whereas timescales range from overall processing duration (minutes) to photostimulated excitation (<nanoseconds) to bond breakage (femtoseconds) (106). To that effect, physics- and chemistry-based modeling has substantially complemented experimental work, contributing tremendously to the understanding of elementary reaction mechanisms that are difficult to examine experimentally (107, 108). Such modeling also has the potential to reduce the time and cost associated with experimental design by allowing prediction of the process outcome. However, the aforementioned range of scales dictates that several different simulation approaches be employed, as no single method is adequate to address the overall scope of this problem. Fundamental principles of fluid mechanics, thermodynamics, and reaction kinetics therefore find varying levels of utility in relation to various facets of the plasma etching process, from reactor continuum to surface reactions, as shown in **Figure 9**. First, thermodynamics provides the foundation for analyzing the respective probabilities of competing mechanisms and forms the basis for molecular dynamic simulation (109–111) atomistic modeling of surfaces exposed to impinging plasma species. At the reactor scale, fluid mechanics govern chamber design considerations such as conductance, pump speed, and flow patterns as well as species transport to and from the surface (112, 113). Finally, in both the gas phase and on the surface, chemical reaction kinetics determine the pathways for etch product formation and the rate-limiting steps of the process (114, 115).

Using the etching of complex metal oxides in halogen chemistry as an example, this section discusses the use of thermodynamics and reaction kinetic theory to develop a robust simulation approach that can be applied to most etching processes. First, however, it is worth pointing out that the selection of plasma chemistry is also driven by other considerations such as environmental concerns, e.g., as most effective gases are halogen based, some of them are major contributors to global warming and are thus undesirable (116, 117). In making a selection, several crucial thermodynamic parameters, shown in **Table 1**, must be considered. At the molecular level, the etching threshold energy of a reaction is strongly correlated to the metal-oxygen bond strength, whereas the difference between metal-oxygen and metal-halogen bond strengths dictates the possible formation of metal halides. The stronger the M–O bonds, the harder it is to initiate or sustain the etching reactions. Following metal-oxygen bond breakage and metal-halogen bond formation, the relative magnitude of the reaction rate coefficients can be determined by comparing the heats of reactions under consideration. By compiling the heats of formation of each reactant and reaction product, the heat of formation under equilibrium can be determined (118) to provide a baseline to assess if a reaction is endothermic or exothermic. However, because plasma is a nonequilibrium

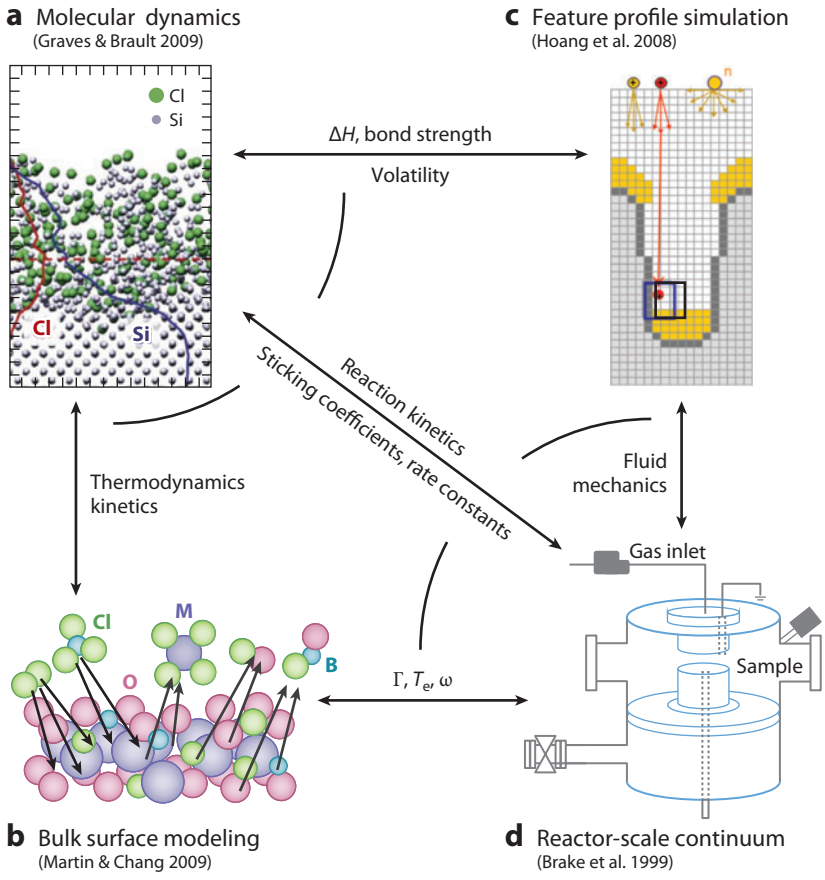


Figure 9

Relationships between fundamental chemical engineering principles (fluid mechanics, thermodynamics, and reaction kinetics) and major components of a plasma etching process. Images adapted from References 143–145.

system, this baseline serves only as a guide; the energetic and reactive species from the plasma usually enable more reactions than equilibrium data suggest. Once the reactions are defined, the volatilities of the reaction products (metal halides) dictate the efficacy of the overall etching reaction; a reaction with more volatile halogenated compounds can be reasonably expected to lead to faster etch rates. Although material safety data sheets usually contain volatility information, a thermodynamics-based approach is often needed to develop volatility diagrams through consideration of the equilibria between condensed and gaseous phases (119). The general approach outlined in **Table 1** involves tabulating such thermodynamic data to comprehensively assess the feasibility of a reaction, which is the first step toward the selection of a plasma chemistry.

After establishing the foundation using the thermodynamic factors discussed above, kinetic studies with the selected chemistry are carried out experimentally to ensure that the model is firmly based on actual observations and to allow for realistic assumptions if simplification is necessary. Measurements of the etch yield/rate, identification and quantification of major etch products, and analysis of the surface composition pre- and post-etch are all useful data sets for comparison

Table 1 Thermodynamic parameters to investigate in selecting viable etch chemistries

Parameter	Example	Value
Bond strength (kJ mol^{-1})	1. $E_{M\text{-}O}$ 2. $E_{M\text{-}X}$	$E_{M-O} < E_{M-X}$ implies higher chance of MX_y formation
ΔH_f (kJ mol^{-1})	1. $M_xO_{y(s)} + (cx + y)X_{(g)} \xrightarrow{\Delta H_1} xMX_{c(g)} + yOX_{(g)}$ 2. $M_xO_{y(s)} + 1/2(cx + y)X_{2(g)} \xrightarrow{\Delta H_2} xMX_{c(g)} + yOX_{(g)}$	$\Delta H_1 < \Delta H_2$ implies higher likelihood of (1) occurring.
Boiling temperature (°C) (volatility)	1. $M_1 \times_1 \rightarrow T_{B1}$ 2. $M_2 \times_1 \rightarrow T_{B2}$ 3. $M_1 \times_2 \rightarrow T_{B3}$	$T_{B1} < T_{B2}$ implies higher etch rate of M_1 over M_2, $T_{B1} < T_{B3}$ implies higher etch rate using X_1 over X_2.

Abbreviations: M, metal; O, oxygen; X, halogen.

when formulating a model of the surface reaction kinetics. Over the past few decades, various phenomenological models have been developed to account for the energy and flux dependencies during plasma etching processes (114, 115, 120–122). A recent development based on a surface site balance approach expanded and combined these models to account for simultaneous etching and deposition by the synergistic reactions of ionic and neutral species on the surface during plasma exposure, as shown in **Table 2** (123). Specifically, etching and deposition rates are balanced on the basis of surface coverage (θ) and parameters including the fluxes of ionic, etching, and depositing species (*J*); sticking probabilities for etching and depositing species (*S*); deposition on the substrate/surface layers (*D*); volume of substrate/surface layer removed or deposited as a function of ion energy and species flux (*v*); and incoming ion, etching threshold, and transition energies (*E*). As the model was built on thermodynamic and kinetic models, its applicability extends from simple binary oxides to complex metal oxides and likely many more materials. However, its broader impact depends on whether it can be used in a feature profile simulator, such as one based on Monte Carlo or similar methods, to enable predictive modeling of feature profile evolution. To properly parameterize the rate coefficients of reaction kinetics, one approach is to convert such a model into a translating mixed layer (TML) format, which is valid because of the ion-induced mixing in the near-surface region (114, 115). A TML model uses a defined set of reactions to predict the etch yield of a process and takes into account the effect of various species present in the plasma as well as different material removal pathways such as sputtering and ion-enhanced etching. Three major reactive fluxes are assumed and balanced: (*a*) the arrival of species to the surface from the gas phase, (*b*) the desorption of species from the surface to the gas phase, and (*c*) the movement from the underlying surface to the mixing layer to compensate for the difference between (*a*) and (*b*). The model estimates etch yield as a function of terms such as ion energy (*E*), neutral/ion fluxes (*J*), angular dependence (φ), sticking probabilities (*S*), and reaction rate coefficients (β). Those parameters that cannot be calculated directly are obtained by fitting the model to experimental data. This model also allows for estimation of the composition of the mixing layer, which may include vacancies generated during etching (*V*), to provide a means of comparison with the surface analysis of etched films. A comparison of the phenomenological and TML models is in **Table 2**. Detailed studies show good agreement between experiments and both models for several high-*k* materials (HfO_2, Al_2O_3, and $Hf_xAl_yO_z$) etched in Cl_2 and BCl_3 plasmas, as shown in **Figure 10**, including direct comparison between experimentally determined and Monte Carlo–simulated profiles (123, 124). This approach has the potential to become the platform for prediction of the etching of even more complex materials, including elements that form less volatile reaction products such as those projected to be implemented in memory devices, e.g., phase change materials and multiferroics.

Table 2 Comparison between two models developed for two typical etching reactions in metal oxides etched in halogen gases: $MO_{2(s)}+3Cl_{2(g)} \rightarrow MCl_{4(g)}+2ClO_{(g)}$ and $MO_{2(s)}+2BCl_{3(g)} \rightarrow MCl_{4(g)}+2BOCl_{(g)}$

Phenomenological Model (125)	Translating Mixed Layer Model (124)	
$DR_s = D_s\theta_{ds} = J_d v_{ds} S_{ds} \theta_1$	$Cl_{(g)} \rightarrow Cl_{(s)}$	$DR_1 = S_{Cl} J_{Cl} x_{M-V}$
$DR_p = D_p\theta_{dp} = J_p v_{dp} S_{dp} \theta_z$	$Cl^+_{(g)} \rightarrow Cl_{(s)}$	$DR_2 = S_{Cl^+} J_{Cl^+}$
$ER_s = J_i\theta_{es}\left[A_s\left(E_{ion}^{\frac{1}{2}} - E_{th,s}^{\frac{1}{2}}\right) + B_s\left(E_{ion}^{\frac{1}{2}} - E_{tr,s}^{\frac{1}{2}}\right)\right] = J_e v_{es} S_{es} \theta_1$	$Cl_{(s)} + O_{(s)} \rightarrow ClO_{(g)}$	$ER_1 = \beta_{ClO}(x_{Cl-O})$
$ER_p = J_i C_p\left(E_{ion}^{\frac{1}{2}} - E_{th,p}^{\frac{1}{2}}\right)\theta_{ep} = J_e v_{ep} S_{ep} \theta_2$	$BCl_{(s)} + O_{(s)} \rightarrow BOCl_{(g)}$	$ER_2 = \beta_{BOCl}(x_{B-Cl})(x_{O-V})$
$\theta_{es} + \theta_{ds} + \theta_{ep} + \theta_{dp} + \theta_1 + \theta_2 = 1$	$M_{(s)} + 4Cl_{(s)} \rightarrow MCl_{4(g)}$	$ER_3 = \beta_{MCl_4}(x_{M-Cl})^4$
$R_t = (ER)_{es} - (DR)_{ds} + (ER)_{ep} - (DR)_{dp}$	$R_M = DR_1 + DR_2 - 2ER_1 - 3ER_2 - 5ER_3$	
$R_t = \begin{pmatrix} J_e^2 Z_{es} Z_{ep} \\ -J_d^2 Z_{ds} Z_{dp} \end{pmatrix} \Big/ \left(\begin{array}{c} J_d Z_{ds} + J_e Z_{ep} + \\ \frac{J_d^2 Z_{ds} Z_{dp}}{D_p} + \frac{J_d J_e Z_{ds} Z_{dp}}{D_s} \\ + \frac{J_d J_e Z_{ds} Z_{dp}}{J_i C_p\left(E_{ion}^{\frac{1}{2}} - E_{th,p}^{\frac{1}{2}}\right)} \\ + \frac{J_e^2 Z_{es} Z_{ep}}{J_i\left[A_s\left(E_{ion}^{\frac{1}{2}} - E_{th,s}^{\frac{1}{2}}\right) + B_s\left(E_{ion}^{\frac{1}{2}} - E_{tr,s}^{\frac{1}{2}}\right)\right]} \end{array} \right)$	$dM/dt = -ER_3$	
	$dO/dt = -ER_1 - ER_2$	
	$dCl/dt = -ER_1 - ER_2 - 4ER_2 + DR_1 + DR_2$	
	$\beta = f(E_{ion}, E_{th}, \varphi)$	
	$R_t = f(S, R, \beta, J, x)$	

Abbreviations: A, B, C, volume removed as a function of ion energy; β, rate coefficient; D, deposition rate; E, energy value of the ion (ion), threshold for etching of substrate (th,s) and polymer (th,p), and transition point for etching of substrate (tr,s); ER/DR, overall etch/deposition rate of substrate (s) and polymer (p); φ, angular dependence; J, fluxes of ionic (i), etching (e), and depositing (d) species; θ, surface coverage; R_t, net etch/deposition rate; v, volume of materials removed or deposited as a function of species flux; x, bond concentration for metal (M), oxygen (O), chlorine (Cl), and vacancies (V); $Z_{\alpha\gamma} = v_{\alpha\gamma} S_{\alpha\gamma}$; S, sticking probability. Only a few selected equations are given as representatives for the translating mixed layer model owing to space constraints.

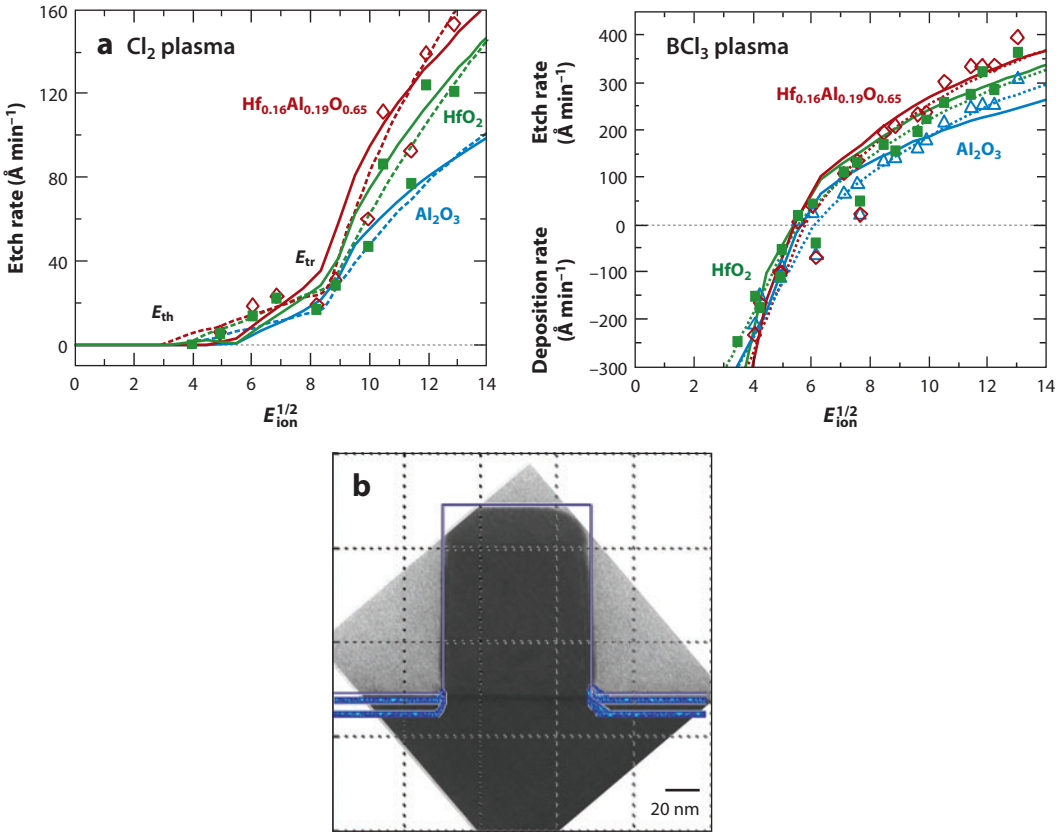


Figure 10

(*a*) Fitting of phenomenological (*dashed line*) and translating mixed layer (TML) (*solid line*) models to etch rate data (123) for HfO_2, Al_2O_3, and $Hf_xAl_yO_z$ films in Cl_2 and BCl_3 plasmas at 500 W and 3 mtorr. (*b*) Comparison of the experimentally measured profile (146) for HfO_2 etched in a Cl_2-based plasma to that simulated by the Monte Carlo method using the TML model (N. Marchack & J.P. Chang, in preparation).

Atomic Layer Etching and Lithography Limits

As novel materials such as complex and multifunctional materials (multiferroics) that are intrinsically harder to etch become more commonly incorporated into device architecture, more aggressive etch chemistries may need to be explored. However, the simultaneous trend of decreasing the critical dimensions of patterned features into the nanometer regime means that a compromise must be made as the margin for error between excessive and insufficient etching becomes much narrower. Atomic layer etching (ALE) is a possible means of addressing this issue (125). In the conventional plasma etch process, the synergism of species in the gas phase as well as on the surface is fully embraced, and a multitude of reactions takes place, which results in a surface that is disrupted and not fully controlled (**Figure 11*a***). In contrast, ALE involves reproducibly removing single atomic layers of a surface through a series of self-limiting etching steps (**Figure 11*b***). If ALD is a layer-by-layer version of a CVD process, ALE can be regarded as a layer-by-layer version of a plasma etching process. Taking advantage of the surface chemistries learned in ALD processes, ALE can be considered a reverse process in that the four main steps are: (*a*) adsorption (chemisorption) of one species onto the surface that self-terminates upon

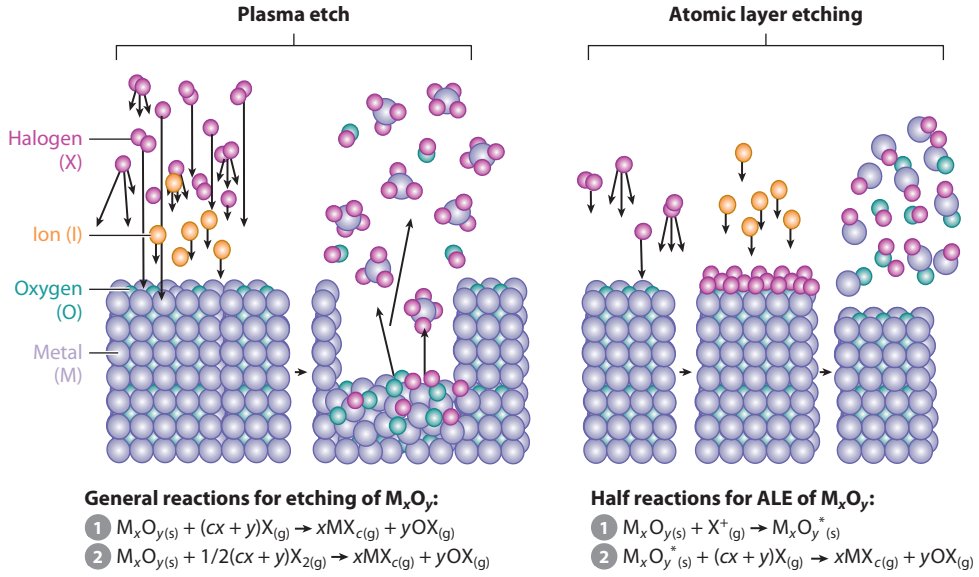


Figure 11

Comparison between a traditional plasma etch process and an atomic layer etching (ALE) process that illustrates the conceptual differences.

consumption of the available surface sites; (*b*) evacuation of the reactor to prevent reaction in the gas phase; (*c*) exposure of the surface to a second species to induce chemical reaction with the adsorbed species, leading to an ALE; and (*d*) evacuation of the reactor to remove the reaction products. The most important factor in achieving atomic-scale control is that at least one of the steps, (*a*) or (*c*), should be self-limiting.

In a plausible ALE process, ions can be the enabling species to form and remove a volatile product. The energy of the ions should be low enough to prevent excessive sputtering but higher than the threshold energy for etching. This general concept has been demonstrated for the etching of silicon (125), germanium (126), and gallium arsenide (127), with only a few minor differences between the three cases. Some recent simulation work (128) has been done, but more thorough experimental work, particularly with regard to different material systems, is greatly needed.

Last but not least, the overall success of a top-down nanopatterning process hinges upon the efficacy of the optical lithography process, especially the optical equipment (e.g., masks, lenses) and photoresist transfer effects (e.g., line edge/width roughness). For the former, the two major challenges are (*a*) promotion of design for manufacturability (DFM) standards to ensure high fidelity and yield of pattern transfers and thus minimize performance degradation, and (*b*) overcoming the inherent limitations put forth by the Rayleigh equation for half-pitch critical dimension, $CD = k_1 \times \lambda/NA$, where k_1 is the process aggressiveness factor, λ is the wavelength of the light used, and NA is the numerical aperture. A two-pronged approach comprising physics-based quantitative assessment of phenomena contributing to transfer defects, such as mask edge effects, defect-feature interactions, and stress-generated variations (129), and techniques such as optical proximity correction (OPC) and off-axis illumination (OAI) has been demonstrated as effective for engineering solutions in the quest to address lithography DFM concerns, as shown in **Figure 12*a*** (130, 131). In addition, much effort has been focused on reducing the value of k_1, by using double-patterning lithography methods such as double exposure-single etch and double exposure-double etch (132),

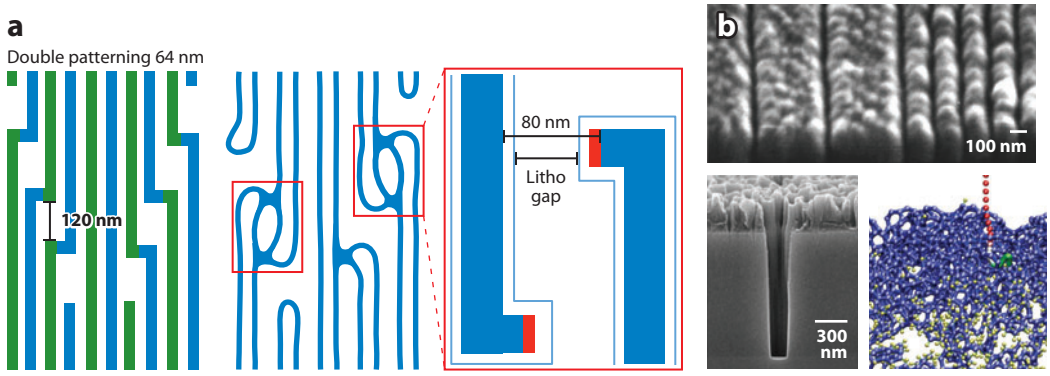


Figure 12

The effect of the plasma-lithography interplay that complicates the patterning fidelity. (*a*) Desired versus obtained features owing to focus, dose, and mask-bias effects. Reprinted from IMEC Scientific Report, "Immersion lithography with double patterning," copyright © 2009, with permission from IMEC. (*b*) Scanning electron microscopy images (147) and molecular dynamics simulation (148) showing line edge and line width roughness caused by photoresist roughening upon Ar^+ ion exposure.

which offers a viable means of reducing printed critical dimensions beyond those of existing single-exposure methods. However, maximizing the quality of the optics-related equipment does not address the potential consequences of plasma interacting with the photoresist layer during the etch process. Owing to the plasma interaction with the photoresist surface and the different chemical moieties in the photoresist, line edge roughness (LER) and line width roughness (LWR) have become much more pronounced as the feature length scale has approached the molecular building block dimension of the photoresist materials. For example, a LWR of less than 2 nm is desired for advanced devices with a feature size less than 30 nm (23). Given that the radius of gyration of the polymers used in photoresist itself is on the order of 2–5 nm, this is clearly a difficult obstacle to surmount. This has led to research to delineate the origin of these effects, such as the ion/vacuum ultraviolet (VUV) photon synergism that resulted in far greater surface roughening than either of the two individual effects (133). Specifically, a cross-linked layer generated by ion bombardment was necessary for roughening to occur, but this layer could be formed only on a surface morphology that had been softened by VUV scission. Additional work has investigated modification of the photoresist composition to suppress LER/LWR both during and after lithographic processing (134, 135), and has modeled both the patterning itself (136, 137) and the deleterious effects on electrical performance (138, 139).

OUTLOOK

Chemical processing of materials on silicon has made an impact far beyond the micro- and nanoelectronic industry: It has enabled technological advancements that are now ubiquitous in our daily lives as well as further scientific discovery and research in the fields of medicine, astronomy, and energy generation. An unprecedented challenge is to design, then synthesize, novel materials that deliver desirable device functionality at a reduced dimensionality and cost. ALD has emerged as a viable and enabling technique to control the distribution, composition, and function of crucial elements in complex materials over large areas and complex 3D surface topography. It also enables interface engineering at the atomic scale that could realize multifunctional heterogeneous superlattices and complex structures. The plasma etching process remains the most reliable method for

nanoscale patterning of high–aspect ratio features and over larger areas. The interplay between lithography and etching is now the limiting factor in extending the efficacy of the top-down patterning process and will necessitate a deeper understanding of the photochemical reactions and their effect on the morphology and evolution of the surfaces. The reversal of ALD surface chemistry to realize ALE has the potential to revolutionize materials synthesis and patterning at the atomic level. Furthermore, chemical processing of materials on silicon holds the promise of an economical and effective platform upon which more functionality and smaller features can be built on much larger wafers.

DISCLOSURE STATEMENT

The authors are not aware of any affiliations, memberships, funding, or financial holdings that might be perceived as affecting the objectivity of this review.

ACKNOWLEDGMENTS

J.P.C. acknowledges the support from the UCLA William F. Seyer Chair and her current and former students, postdoctoral researchers, and collaborators.

LITERATURE CITED

1. Moore EM. 1965. Cramming more components onto integrated circuits. *Electronics* 38(8):114–17
2. Feynman RP. 1960. There's plenty of room at the bottom. *Eng. Sci.* 23:22–36
3. Gunther A, Khan SA, Thalmann M, Trachsel F, Jensen KF. 2004. Transport and reaction in microscale segmented gas-liquid flow. *Lab Chip* 4(4):278–86
4. Burns MA, Johnson BN, Brahmasandra SN, Handique K, Webster JR, et al. 1998. An integrated nanoliter DNA analysis device. *Science* 282(5388):484–87
5. Livak-Dahl E, Sinn I, Burns M. 2011. Microfluidic chemical analysis systems. *Annu. Rev. Chem. Biomol. Eng.* 2:325–53
6. Stone HA, Stroock AD, Ajdari A. 2004. Engineering flows in small devices: microfluidics toward a lab-on-a-chip. *Annu. Rev. Fluid Mech.* 36:381–411
7. Long JW, Dunn B, Rolison DR, White HS. 2004. Three-dimensional battery architectures. *Chem. Rev.* 104(10):4463–92
8. Shao ZP, Haile SM, Ahn J, Ronney PD, Zhan Z, et al. 2005. A thermally self-sustained micro solid-oxide fuel-cell stack with high power density. *Nature* 435(7043):795–98
9. Levitin G, Hess DW. 2011. Surface reactions in microelectronics process technology. *Annu. Rev. Chem. Biomol. Eng.* 2:299–324
10. Derby JJ, Brown RA. 1986. Thermal-capillary analysis of Czochralski and liquid encapsulated Czochralski crystal growth: I. Simulation. *J. Cryst. Growth* 74(3):605–24
11. Falster R, Voronkov VV. 2000. The engineering of intrinsic point defects in silicon wafers and crystals. *Mater. Sci. Eng. B* 73(1–3):87–94
12. Fahey PM, Griffin PB, Plummer JD. 1989. Point-defects and dopant diffusion in silicon. *Rev. Mod. Phys.* 61(2):289–384
13. Weber ER. 1983. Transition metals in silicon. *Appl. Phys. A* 30(1):1–22
14. Seebauer EG, Allen CE. 1995. Estimating surface diffusion coefficients. *Prog. Surf. Sci.* 49(3):265–330
15. Chan K, Gleason KK. 2005. Initiated CVD of poly(methyl methacrylate) thin films. *Chem. Vapor Depos.* 11(10):437–43
16. Wang JG, Mao GP, Ober CK, Kramer EJ. 1997. Liquid crystalline, semifluorinated side group block copolymers with stable low energy surfaces: synthesis, liquid crystalline structure, and critical surface tension. *Macromolecules* 30(7):1906–14

17. Reichmanis E, Houlihan FM, Nalamasu O, Neenan TX. 1991. Chemical amplification mechanisms for microphotolithography. *Chem. Mater.* 3(3):394–407
18. Kern W. 1990. The evolution of silicon-wafer cleaning technology. *J. Electrochem. Soc.* 137(6):1887–92
19. Ohmi T. 1996. Total room temperature wet cleaning for Si substrate surface. *J. Electrochem. Soc.* 143(9):2957–64
20. Jensen KF, Graves DB. 1983. Modeling and analysis of low-pressure CVD reactors. *J. Electrochem. Soc.* 130(9):1950–57
21. Deshmukh SC, Aydil ES. 1995. Investigation of SiO_2 plasma-enhanced chemical-vapor-deposition through tetraethoxysilane using attenuated total-reflection Fourier transform infrared spectroscopy. *J. Vac. Sci. Technol. A* 13(5):2355–67
22. Banerjee S, Cole JV, Jensen KF. 1998. Nonlinear model reduction strategies for rapid thermal processing systems. *IEEE Trans. Semicond. Manuf.* 11(2):266–75
23. Semicond. Ind. Assoc. 2009. International Technology Roadmap for Semiconductors. Austin, TX: SEMATECH
24. Peters MS, Timmerhaus KD, West RE. 2004. *Plant Design and Economics for Chemical Engineers*. New York: McGraw-Hill
25. Dennard RH, Gaensslen FH, Rideout VL, Bassous E, LeBlanc AR. 1974. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE J. Solid-State Circuits* 9:256–68
26. Thompson SE, Chau RS, Ghani T, Mistry K, Tyagi S, Bohr MT. 2005. In search of "forever," continued transistor scaling one new material at a time. *IEEE Trans. Semicond. Manuf.* 18(1):26–36
27. Thompson SE, Armstrong M, Auth C, Cea S, Chau R, et al. A logic nanotechnology featuring strained-silicon. *IEEE Electron Device Lett.* 25(4):191–93
28. Wilk GD, Wallace RM, Anthony JM. 2001. High-κ gate dielectrics: current status and materials properties considerations. *J. Appl. Phys.* 89(10):5243–75
29. Mistry K, Allen C, Auth C, Beattie B, Bergstrom D, et al. 2007. A 45 nm logic technology with high-k + metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging. *Proc. IEEE Int. Electron Devices Meet. '07, Washington, DC*, pp. 247–50. Piscataway, NJ: IEEE
30. Doyle BS, Datta S, Doczy M, et al. 2003. High performance fully-depleted tri-gate CMOS transistors. *IEEE Electron Device Lett.* 24(4):263–65
31. Tans SJ, Verschueren ARM, Dekker C. 1998. Room-temperature transistor based on a single carbon nanotube. *Nature* 393(6680):49–52
32. Horowitz G. 1998. Organic field-effect transistors. *Adv. Mater.* 10(5):365–77
33. Newnham RE. 2005. *Properties of Materials: Anisotropy, Symmetry, Structure*. New York: Oxford Univ. Press
34. Streiffer SK, Eastman JA, Fong DD, Thompson C, Munkholm A, et al. 2002. Observation of nanoscale 180° stripe domains in ferroelectric $PbTiO_3$ thin films. *Phys. Rev. Lett.* 89(6):067601
35. Ahn CH, Rabe KM, Triscone JM. 2004. Ferroelectricity at the nanoscale: local polarization in oxide thin films and heterostructures. *Science* 303(5657):488–91
36. Wang ZL, Song JH. 2006. Piezoelectric nanogenerators based on zinc oxide nanowire arrays. *Science* 312(5771):242–46
37. Wang X, Song J, Liu J, Wang ZL. 2007. Direct-current nanogenerator driven by ultrasonic waves. *Science* 316(5821):102–5
38. Kimura T, Goto T, Shintani H, Ishizaka K, Arima T, et al. 2003. Magnetic control of ferroelectric polarization. *Nature* 426(6962):55–58
39. McKee RA, Walker FJ, Chisholm MF. 2001. Physical structure and inversion charge at a semiconductor interface with a crystalline oxide. *Science* 293:468–71
40. Meindl JD, Chen Q, Davis JA. 2001. Limits on silicon nanoelectronics for terascale integration. *Science* 293(5537):2044–49
41. Polman A. 1997. Erbium implanted thin film photonic materials. *J. Appl. Phys.* 82(1):1–39
42. Wang ZL. 2004. Zinc oxide nanostructures: growth, properties and applications. *J. Phys. Condens. Matter* 16(25):R829–58

43. Liu AS, Jones R, Liao L, Samara-Rubio D, Rubin D, et al. 2004. A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor. *Nature* 427(6975):615–18
44. Law M, Sirbuly DJ, Johnson JC, Goldberger J, Saykally RJ, et al. 2004. Nanoribbon waveguides for subwavelength photonics integration. *Science* 305(5688):1269–73
45. Wolf SA, Awschalom DD, Buhrman RA, Daughton JM, von Molnár S, et al. 2001. Spintronics: a spin-based electronics vision for the future. *Science* 294:1488–95
46. Pearton SJ, Abernathy CR, Overberg ME, Thaler GT, Norton DP, et al. 2003. Wide band gap ferromagnetic semiconductors and oxides. *J. Appl. Phys.* 93(1):1–13
47. Comini E, Faglia G, Sberveglieri G, Pan Z, Wang ZL, et al. 2002. Stable and highly sensitive gas sensors based on semiconducting oxide nanobelts. *Appl. Phys. Lett.* 81(10):1869–71
48. Saito Y, Takao H, Tani T, Tani T, Nonoyama T, Takatori K, et al. 2004. Lead-free piezoceramics. *Nature* 432(7013):84–87
49. Martin LW, Chu YH, Ramesh R. 2010. Advances in the growth and characterization of magnetic, ferroelectric, and multiferroic oxide thin films. *Mater. Sci. Eng. R* 68:89–133
50. Nan C. 2008. Multiferroic magnetoelectric composites: historical perspective, status, and future directions. *J. Appl. Phys.* 103:031101
51. Izyumskaya N, Alivov Y, Morkoç H. 2009. Oxides, oxides, and more oxides: high-κ oxides, ferroelectrics, ferromagnetics, and multiferroics. *Crit. Rev. Solid State Mater. Sci.* 34:89–179
52. Ramesh R, Schlom DG. 2008. Whither oxide electronics? *MRS Bull.* 33:1006–14
53. Lo SH, Buchanan DA, Taur Y, Wang W. 1997. Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's. *IEEE Electron Device Lett.* 18(5):209–11
54. Hubbard KJ, Schlom DG. 1996. Thermodynamic stability of binary oxides in contact with silicon. *J. Mater. Res.* 11(11):2757–76
55. Liu J, Martin RM, Chang JP. 2008. Characteristics of Hf-silicate thin films synthesized by plasma enhanced atomic layer deposition. *J. Vac. Sci. Technol. A* 26(5):1251–57
56. Wilk GD, Wallace RM, Anthony JM. 2000. Hafnium and zirconium silicates for advanced gate dielectrics. *J. Appl. Phys.* 87(1):484–92
57. Robertson J. 2006. High dielectric constant gate oxides for metal oxide Si transistors. *Rep. Prog. Phys.* 69(2):327–96
58. Ho MY, Gong H, Wilk GD, Busch BW, Green ML, et al. 2002. Suppressed crystallization of Hf-based gate dielectrics by controlled addition of Al_2O_3 using atomic layer deposition. *Appl. Phys. Lett.* 81(22):4218–20
59. Yu HY, Wu N, Li MF, Zhu C, Cho BJ, et al. 2002. Thermal stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si. *Appl. Phys. Lett.* 81(19):3618–20
60. Dimoulas A, Vellianitis G, Mavrou G, Apostopoulos G, Travlos A, et al. 2004. $La_2Hf_2O_7$ high-κ gate dielectric grown directly on Si(001) by molecular-beam epitaxy. *Appl. Phys. Lett.* 85(15):3205–207
61. Choi JH, Mao Y, Chang JP. 2011. Development of hafnium based high-*k* materials—a review. *Mater. Sci. Eng. R* 72:97–136
62. Choi CH, Rhee SJ, Jeon TS, Lu N, Sim JH, et al. 2002. Thermally stable CVD HfO_xN_y advanced gate dielectrics with poly-Si gate electrode. *Int. Electron Devices Meet. Tech. Dig., San Francisco*, pp. 857–60. Piscataway, NJ: IEEE
63. Kang CS, Cho HJ, Choi R, Kim YH, Kang CY, et al. 2004. The electrical and material characterization of hafnium oxynitride gate dielectrics with TaN-gate electrode. *IEEE Trans. Electron Devices* 51(2):220–27
64. Eerenstein W, Mathur ND, Scott JF. 2006. Multiferroic and magnetoelectric materials. *Nature* 442:759–65
65. Schmid H. 1994. Multi-ferroic magnetoelectrics. *Ferroelectrics* 162:317–38
66. Jia C. 2009. Multiferroic oxides-based flash memory and spin-field-effect transistor. *Appl. Phys. Lett.* 95:012105
67. Chu YH, Martin LW, Holcomb MB, Gajek M, Shu Jen H, et al. 2008. Electric-field control of local ferromagnetism using a magnetoelectric multiferroic. *Nat. Mater.* 7:478–82
68. Scott JF. 2007. Data storage: multiferroic memories. *Nat. Mater.* 6:256–57
69. Ahn SE, Lee MJ, Park Y, Kang BS, Lee CB, et al. 2008. Write current reduction in transition metal oxide based resistance-change memory. *Adv. Mater.* 20(5):924–28

70. Wang J, Neaton JB, Zheng H, Nagarajan V, Ogale SB, et al. 2003. Epitaxial $BiFeO_3$ multiferroic thin film heterostructures. *Science* 299:1719–22
71. Kuo HY, Slinger A, Bhattacharya K. 2010. Optimization of magnetoelectricity in piezoelectric-magnetostrictive bilayers. *Smart Mater. Struct.* 19:125010
72. Fechner M, Maznichenko IV, Ostanin S, Ernst A, Henk J, Mertig I. 2010. Ab initio study of magnetoelectricity in composite multiferroics. *Phys. Status Solidi* (*b*) 247:1600–7
73. Srinivas A, Karthik T, Gopalan R, Chandrasekaran V. 2010. Improved magnetoelectricity by uniaxial magnetic field pressed and sintered composites in $BaTiO_{3(x)}$-$BaFe_{12}O_{19(1-x)}$ system ($x = 0.8, 0.6$). *Mater. Sci. Eng. B* 172:289–93
74. Avellaneda M, Harshe G. 1994. Magnetoelectric effect in piezoelectric magnetostrictive multilayer (2–2) composites. *J. Intell. Mater. Syst. Struct.* 5:501–13
75. Bichurin MI, Petrov VM, Srinivasan G. 2003. Theory of low-frequency magnetoelectric coupling in magnetostrictive-piezoelectric bilayers. *Phys. Rev. B* 68:054402
76. Zheng H, Wang J, Lofland SE, Ma Z, Mohaddes-Ardabili L, et al. 2004. Multiferroic $BaTiO_3$-$CoFe_2O_4$ nanostructures. *Science* 303:661–63
77. Dix N, Muralidharan R, Rebled J-M, Estrade S, Peiro F, et al. 2010. Selectable spontaneous polarization direction and magnetic anisotropy in $BiFeO_3$-$CoFe_2O_4$ epitaxial nanostructures. *ACS Nano* 4:4955–61
78. Liu M. 2007. A modified sol-gel process for multiferroic nanocomposite films. *J. Appl. Phys.* 102:083911
79. Suntola T. 1996. Surface chemistry of materials deposition at atomic layer level. *Appl. Surf. Sci.* 100:391–98
80. Kattelus H, Ylilammi M, Saarilahti J, Antson J, Lindfors S. 1993. Layered tantalum-aluminum oxide-films deposition by atomic layer epitaxy. *Thin Solid Films* 225:296–98
81. Chang JP. 2005. High-K gate dielectric deposition technology survey. In *High-K Gate Dielectric Materials for VLSI MOSFET*, ed. HR Huff, DC Gilmer, pp. 379–407. Berlin: Springer-Verlag
82. Leskela M, Ritala M. 2002. Atomic layer deposition (ALD): from precursors to thin film structures. *Thin Solid Films* 409:138–46
83. Sneh O, Clark-Phelps RB, Londergan AR, Winkler J, Seidel TE. 2002. Thin film atomic layer deposition equipment for semiconductor processing. *Thin Solid Films* 402:248–61
84. Ritala M, Leskela M. 2002. Atomic layer deposition. In *Handbook of Thin Film Materials*, ed. HS Nalwa, 1:103–56, San Diego: Academic
85. Klaus JW, Sneh O, George SM. 1997. Growth of SiO_2 at room temperature with the use of catalyzed sequential half-reactions. *Science* 278:1934–36
86. Lin YS, Puthenkovilakam R, Chang JP. 2002. Dielectric property and thermal stability of HfO_2 on silicon. *Appl. Phys. Lett.* 81(11):2041–43
87. Elam JW, Sechrist ZA, George SM. 2002. ZnO/Al_2O_3 nanolaminates fabricated by atomic layer deposition: growth and surface roughness measurements. *Thin Solid Films* 414(1):43–55
88. Granneman E, Fischer P, Pierreux D, Terhorst H, Zagwijn P. 2007. Batch ALD: characteristics, comparison with single wafer ALD, and examples. *Surf. Coat. Technol.* 201(22–23):8899–907
89. Van TT, Chang JP. 2005. Surface reaction kinetics of metal β-diketonate precursors with O radicals in radical-enhanced atomic layer deposition of metal oxides. *Appl. Surf. Sci.* 246(1–3):250–61
90. Van TT, Chang JP. 2005. Controlled erbium incorporation and photoluminescence of Er-doped Y_2O_3. *Appl. Phys. Lett.* 87(1):011907
91. Zhang F, Perng YC, Choi JH, Wu T, Chung TK, et al. 2011. Atomic layer deposition of $Pb(Zr,Ti)O_x$ on 4H-SiC for metal-ferroelectric-insulator-semiconductor diodes. *J. Appl. Phys.* 109:124109
92. Quickel TE, Le VH, Brezesinski T, Tolbert SH. 2010. On the correlation between nanoscale structure and magnetic properties in ordered mesoporous cobalt ferrite ($CoFe_2O_4$) thin films. *Nano Lett.* 10(8):2982–88
93. Flamm DL, Donnelly VM, Ibbotson DE. 1983. Basic chemistry and mechanisms of plasma etching. *J. Vac. Sci. Technol. B* 1(1):23–30
94. Ventzek PLG, Hoekstra RJ, Kushner MJ. 1994. Two-dimensional modeling of high plasma density inductively coupled sources for materials processing. *J. Vac. Sci. Technol. B* 12(1):461–77
95. Chen R, Bent SF. 2006. Chemistry for positive pattern transfer using area-selective atomic layer deposition. *Adv. Mater.* 18(8):1086–90

96. Liu J, Mao Y, Lan E, Banatao DR, Forse GJ, et al. 2008. Generation of oxide nanopatterns by combining self-assembly of S-layer proteins and area selective atomic layer deposition. *J. Am. Chem. Soc.* 130(50):16908–13
97. Kastenmeier BEE, Matsuo PJ, Beulens JJ, Oehrlein GS. 1996. Chemical dry etching of silicon nitride and silicon dioxide using $CF_4/O_2/N_2$ gas mixtures. *J. Vac. Sci. Technol. A* 14:2802–13
98. Coburn JW, Winters HF. 1979. Ion-assisted and electron assisted gas-surface chemistry—an important effect in plasma etching. *J. Appl. Phys.* 50(5):3189–96
99. Chang JP, Coburn JW. 2003. Plasma-surface interactions. *J. Vac. Sci. Technol. A* 21(5):S145–51
100. Lill T, Joubert O. 2008. Materials science–the cutting edge of plasma etching. *Science* 319:1050–51
101. Jung KB, Cho H, Hahn YB, Lambers ES, Onishi S, et al. 1999. Relative merits of Cl_2 and CO/NH_3 plasma chemistries for dry etching of magnetic random access memory device elements. *J. Appl. Phys.* 85:4788–90
102. Barone ME, Graves DB. 1996. Molecular dynamics simulations of plasma-surface chemistry. *Plasma Sources Sci. Technol.* 5(2):187–92
103. Lymberopoulos DP, Economou DJ. 1993. Fluid simulations of radio-frequency glow discharges: two-dimensional argon discharge including metastables. *Appl. Phys. Lett.* 63(18):2478–80
104. Frenklach M. 1998. Simulation of surface reactions. *Pure Appl. Chem.* 70(2):477–84
105. Vepřek S. 1972. Statistical model of chemical reactions in nonisothermal low-pressure plasma. *J. Chem. Phys.* 57(2):952–59
106. Rosker MJ, Dantus M, Zewail AH. 1988. Femtosecond clocking of the chemical bond. *Science* 241:1200–2
107. Edelberg EA, Aydil ES. 1999. Modeling of the sheath and the energy distribution of ions bombarding rf-biased substrates in high density plasma reactors and comparison to experimental measurements. *J. Appl. Phys.* 86(9):4799–812
108. Stewart RA, Vitello P, Graves DB. 1994. Two-dimensional fluid model of high density inductively coupled plasma sources. *J. Vac. Sci. Technol. B* 12(1):478–85
109. Helmer BA, Graves DB. 1998. Molecular dynamics simulations of Ar^+ and Cl^+ impacts onto silicon surfaces: distributions of reflected energies and angles. *J. Vac. Sci. Technol. A* 16:3502–14
110. Rauf S, Sparks T, Ventzek PLG, Smirnov VV, Stengach AV, et al. 2007. A molecular dynamics investigation of fluorocarbon based layer-by-layer etching of silicon and SiO_2. *J. Appl. Phys.* 101:033308
111. Barone ME, Robinson TO, Graves DB. 1996. Molecular dynamics simulations of direct reactive ion etching: surface roughening of silicon by chlorine. *IEEE Trans. Plasma Sci.* 24:77–78
112. Hsu CC, Coburn JW, Graves DB. 2006. Etching of ruthenium coatings in O_2- and Cl_2-containing plasmas. *J. Vac. Sci. Technol. A* 24:1–8
113. Hsu CC, Titus MJ, Graves DB. 2007. Measurement and modeling of time- and spatial-resolved wafer surface temperature in inductively coupled plasmas. *J. Vac. Sci. Technol. A* 25:607–14
114. Kwon O, Sawin HH. 2006. Surface kinetics modeling of silicon and silicon oxide plasma etching. II. Plasma etching surface kinetics modeling using translating mixed-layer representation. *J. Vac. Sci. Technol. A* 24:1914–19
115. Kwon O, Bai B, Sawin HH. 2006. Surface kinetics modeling of silicon and silicon oxide plasma etching. III. Modeling of silicon oxide etching in fluorocarbon chemistry using translating mixed-layer representation. *J. Vac. Sci. Technol. A* 24:1920–27
116. Raoux S, Tanaka T, Bhan M, Ponnekanti H, Seamons M, et al. 1999. Remote microwave plasma source for cleaning chemical vapor deposition chambers: technology for reducing global warming gas emissions. *J. Vac. Sci. Technol. B* 17(2):477–85
117. Roehl CM, Boglu D, Bruhl C, Moortgat GK. 1995. Infrared band intensities and global warming potentials of CF_4, C_2F_6, C_3F_8, C_4F_{10}, C_5F_{12}, and C_6F_{14}. *Geophys. Res. Lett.* 22(7):815–18
118. McNevin SC. 1986. Chemical etching of GaAs and InP by chlorine—the thermodynamically predicted dependence on Cl_2 pressure and temperature. *J. Vac. Sci. Technol. B* 4:1216–26
119. Kulkarni NS, DeHoff RT. 2002. Application of volatility diagrams for low temperature, dry etching, and planarization of copper. *J. Electrochem. Soc.* 149:G620–32
120. Mayer TM, Barker RA. 1982. Simulation of plasma-assisted etching processes by ion-beam techniques. *J. Vac. Sci. Technol.* 21(3):757–63

121. Steinbruchel C. 1989. Universal energy dependence of physical and ion-enhanced chemical etch yields at low ion energy. *Appl. Phys. Lett.* 55(19):1960–62
122. Ding J, Hershkowitz N. 1996. Symmetric rate model for fluorocarbon plasma etching of SiO_2. *Appl. Phys. Lett.* 68(12):1619–21
123. Martin RM, Chang JP. 2009. Plasma etching of Hf-based high-*k* thin films. Part III. Modeling the reaction mechanisms. *J. Vac. Sci. Technol. A* 27(2):224–29
124. Marchack NP, Pham C, Hoang J, Chang JP. 2010. *Predicting the surface response upon simultaneous plasma etching and deposition.* Presented at Am. Vac. Soc. Int. Symp., 57th, Albuquerque
125. Athavale SD, Economou DJ. 1996. Realization of atomic layer etching of silicon. *J. Vac. Sci. Technol. B* 14:3702–5
126. Sugiyama T, Matsuura T, Murota J. 1997. Atomic-layer etching of Ge using an ultraclean ECR plasma. *Appl. Surf. Sci.* 112:187–90
127. Lim WS, Park SD, Park BJ, Yeom GY. 2008. Atomic layer etching of (100)/(111) GaAs with chlorine and low angle forward reflected Ne neutral beam. *Surf. Coat. Technol.* 202:5701–4
128. Agarwal A, Kushner MJ. 2009. Plasma atomic layer etching using conventional plasma equipment. *J. Vac. Sci. Technol. A* 27:37–50
129. Neureuther A. 2010. *Measuring, understanding and controlling variability in deep sub-micron patterning*. Presented at Integr. Model., Process, Comput. Technol. Biannu. Workshop, 5th, San Jose, CA
130. Gupta P, Kahng AB, Park CH. 2007. Detailed placement for enhanced control of resist and etch CDs. *IEEE Trans. Comp. Aided Des. Integr. Circuits Syst.* 26:2144–57
131. Gupta P, Kahng AB, Park CH, Samadi K, Xu X. 2006. Wafer topography-aware optical proximity correction. *IEEE Trans. Comp. Aided Des. Integr. Circuits Syst.* 25:2747–56
132. Ronse K, Jansen P, Gronheid R, Hendrickx E, Maenhoudt M, et al. 2009. Lithography options for the 32 nm half pitch node and beyond. *IEEE Trans. Circuits Syst. I* 56:1884–91
133. Titus MJ, Nest DG, Chung TY, Graves DB. 2009. Comparing 193 nm photoresist roughening in an inductively coupled plasma system and vacuum beam system. *J. Phys. D* 42(24):245205
134. Kim SH, Hiroshima H, Komuro M. 2006. Photo-nanoimprint lithography combined with thermal treatment to improve resist pattern line-edge roughness. *Nanotechnology* 17:2219–22
135. Padmanaban M, Rentkiewicz D, Hong C, Lee D, Rahman D, et al. 2005. Possible origins and some methods to minimize LER. *J. Photopolym. Sci. Technol.* 18(4):451–56
136. Oldham WG, Neureuther AR, Sung C, Reynolds JL, Nandgaonkar SN. 1980. A general simulator for VLSI lithography and etching processes: part 2—application to deposition and etching. *IEEE Trans. Electron Devices* 27:1455–59
137. Wong AK, Neureuther AR. 1995. Rigorous 3-dimensional time-domain finite-difference electromagnetic simulation for photolithographic applications. *IEEE Trans. Semicond. Manuf.* 8(4):419–31
138. Deng YF, Neureuther AR. 2003. Electromagnetic characterization of nanoimprint mold inspection. *J. Vac. Sci. Technol. B* 21:130–34
139. Diaz CH, Tao HJ, Ku YC, Yen A, Young K. 2001. An experimentally validated analytical model for gate line-edge roughness (LER) effects on technology scaling. *IEEE Electron Device Lett.* 22:287–89
140. Watanabe M, Kramer S. 2006. 450 mm silicon: an opportunity and wafer scaling. *Electrochem. Soc. Interface* 15(4):28–31
141. Khomskii D. 2009. Classifying multiferroics: mechanisms and effects. *Physics* 2:20
142. Marchack N, Chang JP. 2011. Perspectives in nanoscale plasma etching: what are the ultimate limits? *J. Phys. D* 44:174011
143. Graves DB, Brault P. 2009. Molecular dynamics for low temperature plasma-surface interaction studies. *J. Phys. D* 42(19):194011
144. Hoang J, Hsu CC, Chang JP. 2008. Feature profile evolution during shallow trench isolation etch in chlorine-based plasmas. I. Feature scale modeling. *J. Vac. Sci. Technol. B* 26(6):1911–18
145. Brake ML, Pender J, Fournier J. 1999. The Gaseous Electronic Conference (GEC) reference cell as a benchmark for understanding microelectronics processing plasmas. *Phys. Plasmas* 6(5):2307–13
146. Mangiagalli P, Lill T. 2006. Plasma etching of HfO_2 at elevated temperatures in chlorine-based chemistry. *J. Vac. Sci. Technol. A* 24(1):30–40

147. Oehrlein GS, Phaneuf RJ, Graves DB. 2011. Plasma-polymer interactions: a review of progress in understanding polymer resist mask durability during plasma etching for nanoscale fabrication. *J. Vac. Sci. Technol. B* 29(1):010801
148. Vegh JJ, Graves DB. 2009. Molecular dynamics simulations of Ar^+-organic polymer interactions. *Plasma Process. Polym.* 6:320–34

Annual Review of Chemical and Biomolecular Engineering

Volume 3, 2012

Contents

Indexes

Errata

An online log of corrections to *Annual Review of Chemical and Biomolecular Engineering* articles may be found at http://chembioeng.annualreviews.org/errata.shtml